12 GHz SATELLITE VIDEO RECEIVER

LOW NOISE, LOW COST PROTOTYPE MODEL FOR TV RECEPTION FROM BROADCASTING SATELLITES

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PREFACE

The objective of this effort was to develop a 12 GHz receiver for reception of FM television signals from broadcasting satellites. The receiver is to provide both low noise performance and low cost in production quantities of 1000 units. The progam goal was to have a maximum noise figure of 4 dB and an estimated maximum selling price of $1,000 in quantities of 1,000.

The program included a design phase, a prototype development phase, and a pricing phase to determine an estimated cost for the resulting production receivers in quantities of 10, 100, and 1,000 units.

The receiver developed can receive at any of the 12 transponder frequencies in the 11.7-12.2 GHz range and consists of two packages, an outdoor downconverter unit, which is mounted directly on the receive antenna feed waveguide flange, and an indoor demodulator unit positioned near a video monitor. The receiver subsystems have implemented technology consistent with performance and price constraints. These include, in the outdoor unit, a low noise 12 GHz FET preamplifier, a microstrip branchline coupled balanced mixer, a 10.75 GHz Gunn diode cavity oscillator, and a low noise bipolar IF amplifier. The indoor unit subsystems include a microstrip tuner section, a phase locked threshold extension demodulator, and digital channel select logic.

The developed receiver prototype meets or exceeds all video and audio performance goals. The estimated production cost for this present prototype excluding profit and tooling costs, in 1,000 lot quantities, is greater than $1,000 by $540. However, as explained in the text a number of tradeoffs and design modifications can be implemented to reduce this cost to below $1,000. Low cost is best achieved with use of integrated

assemblies for the downconverter and for the tuning logic. These developments are feasible only when the quantity requirements are greater than 100,000 units.

Design tradeoffs and modifications are included in the production pricing to show their impact on price reduction. Production pricing is also quite dependent on total test time and efficient testing schemes will be pointed out which further aid in price reduction. Since the receiver packaging is quite modular, it is readily adaptible to ease of field repair.

The work performed under this contract has resulted in the development of a 12 GHz satellite receiver design which can be mass produced at a cost under $1540 without sacrificing system performance. The receiver also has the capability of selecting any of the twelve assigned satellite broadcast channels in the frequency range between 11.7 to 12.2 GHz.

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1.0 RECEIVER DESCRIPTION AND PERFORMANCE

1.1 FUNCTIONAL DESCRIPTION

The developed receiver is a 12 channel synchronous phase lock video receiver for reception from broadcast satellites. It accepts a frequency modulated video signal, with audio subcarrier, in the frequency range 11.7-12.2 GHz and provides a 1 Vp-p demodulated video plus a separate audio output signal at a 0 dBm level.

The receiver is compatible for reception of standard 525 line video per CCIR Rec. 405-1. The received RF format contains a frequency modulated video signal with a baseband bandwidth of 4.2 MHz and peak deviation of 10.0 MHz, and a frequency modulated audio signal with a subcarrier frequency of 5.14 MHz, peak deviation (C by SC) of 630 KHz, subcarrier bandwidth of 160 KHz, audio bandwidth of 15 KHz, and peak deviation of 60.0 KHz.

The receiver consists of an Outdoor Downconverter Unit and an Indoor Demodulator Unit. The two units are interconnected by a RF cable, up to 100 feet in length, for transmission of the downconverted signal from the outdoor unit to the indoor unit, and by a four wire power line, for power transmission from the indoor unit to the outdoor unit.

The Downconverter unit is housed in a weatherproof assembly and is mounted directly on the receive antenna feed waveguide flange. A picture of the unit is shown in Figure 1-1 and its block diagram is shown in Figure 1-2.

The unit face plate contains the RF input waveguide port (WR 75), the IF output type "F" female receptacle, the four pin power supply input connector, and monitor jacks for measuring received signal strength.

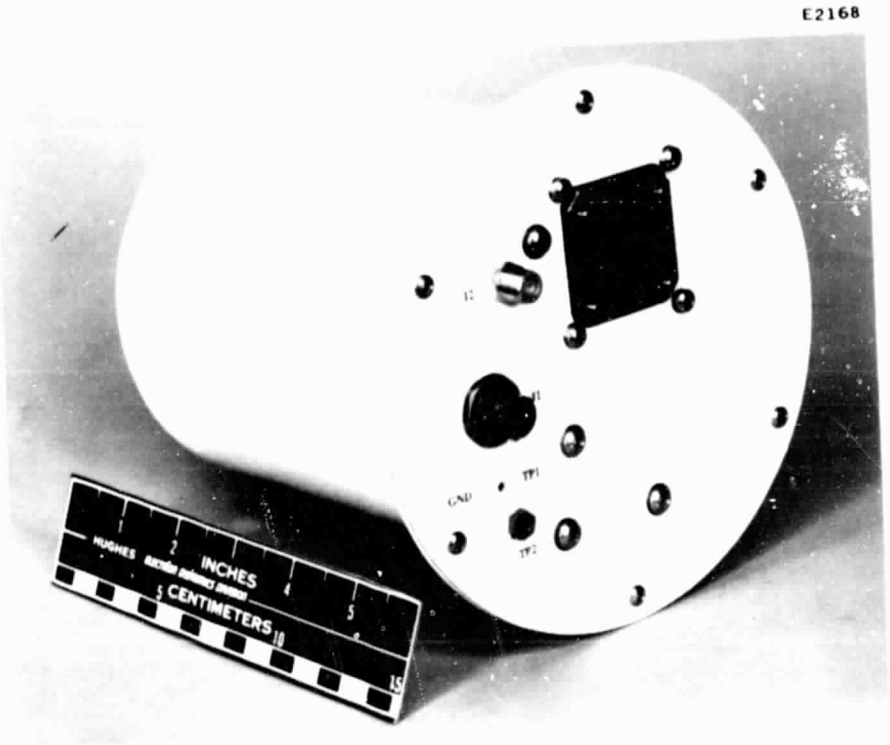

Figure 1-1 Outdoor unit.

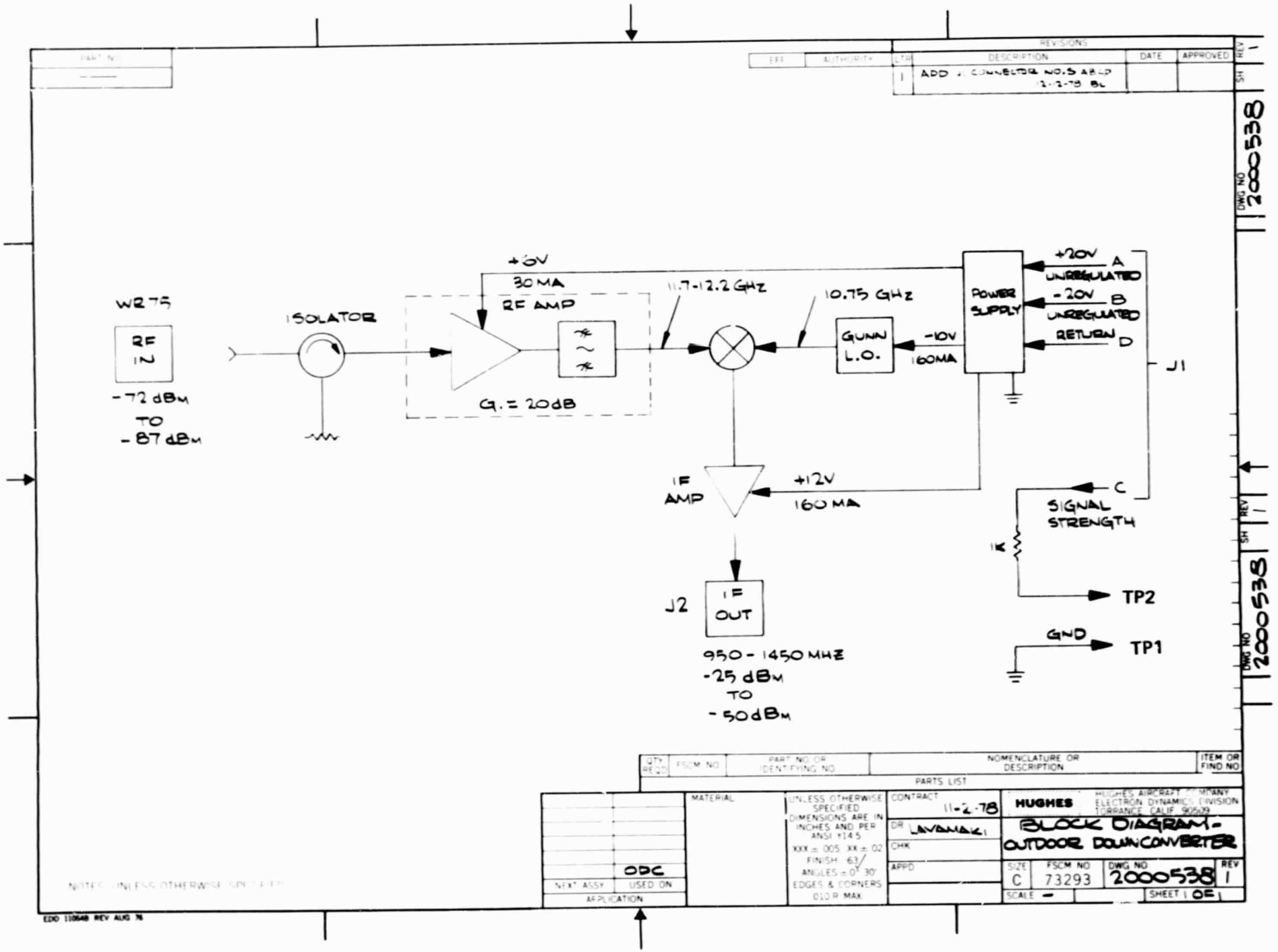

Figure 1-2 Outdoor unit, block diagram.

The signal strength indication is an aid in positioning the antenna for optimum signal reception.

The downconverter operation is specified for a RF input power in the range of -72 to -87 dBm between 11.73 GHz to 12.17 GHz in increments of 40 MHz. The RF input is sent through a waveguide isolator and a waveguide to coaxial adapter, then into the low noise GaAs FET RF amplifier and bandpass filter. The RF amplifier is a three stage amplifier utilizing 0.5 μm gate length FETs and provides a nominal noise figure of 3.4 dB with 21 dB gain.

Contained in the housing with the FET amplifier is a microstrip bandpass filter (BPF) which selects the 11.7-12.2 GHz portion of the incoming signal and feeds the signal to the branchline coupled balanced microstrip mixer. The BPF also provides image rejection for the mixer. The mixer local oscillator is a Gunn diode cavity oscillator with a stable output at 10.75 $\pm$ 0.004 GHz. The IF output of the mixer, at 950 to 1450 MHz, is then sent to the four stage IF amplifier. The total RF to IF gain of the downconverter unit is nominally 52 dB.

The cable interconnections between the Outdoor and Indoor Units consists of a 100 foot long low cost RF cable with approximately 13 dB loss, and a four wire 100 foot long power supply cable carrying plus and minus unregulated voltages, power supply return, and signal strength indicator level.

The downconverted RF signal at 950 to 1450 MHz is received by the Indoor Demodulator Unit, which will typically be stationed near a TV monitor. A picture of this unit is shown in Figure 1-3 and its block diagram is shown in Figure 1-4. The input signal is first routed to the microstrip tuner board. This board consists of three shielded sections, a RF amplifier and bandpass filter, a local oscillator, low pass filter, and mixer, and an IF amplifier and IF band pass filter. The input RF

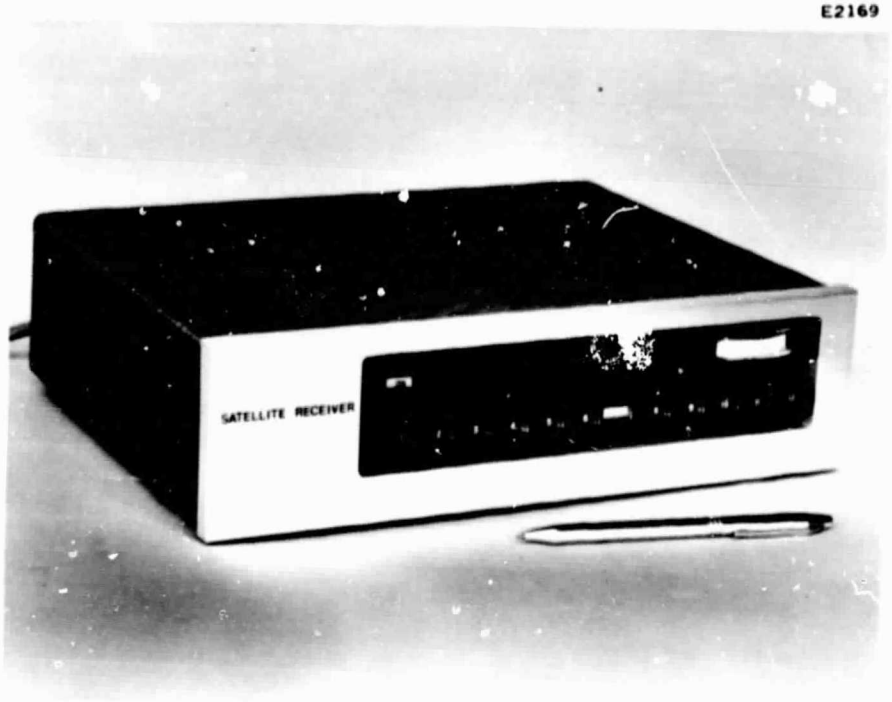

Figure 1-3A Indoor unit.

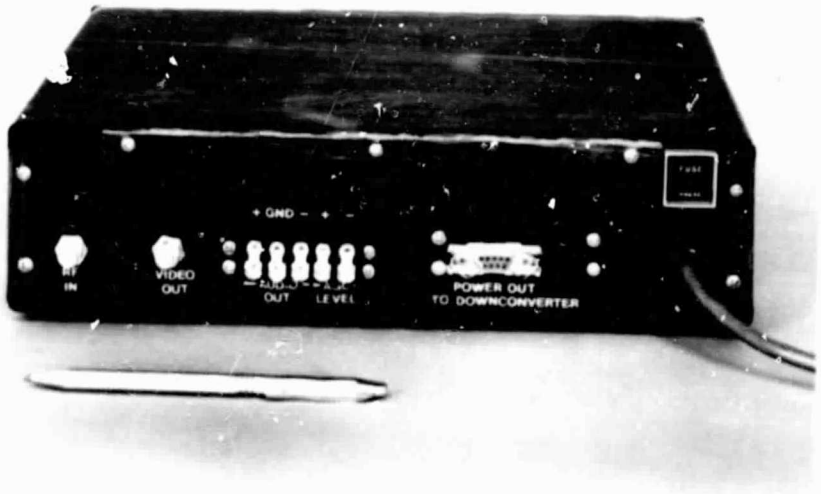

Figure 1-3B Indoor unit.

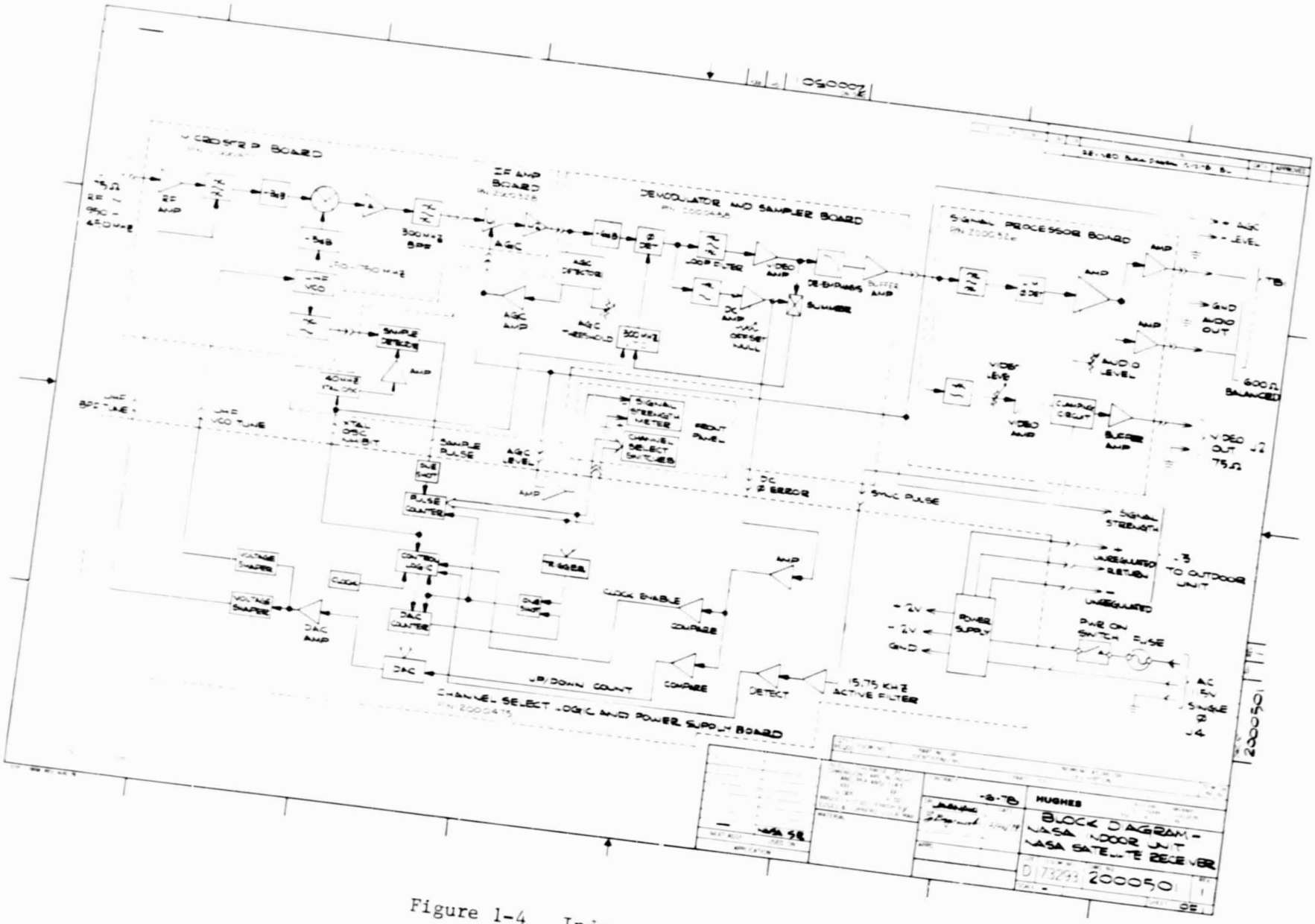

Figure 1-4 Indoor unit, block diagram.

signal if first amplified and then filtered by the tunable band pass filter (BPF) which is controlled by the channel select logic board. The tunable BFP has a nominal bandwidth of 200 MHz and is required to reject those video channels which may interfere with the selected channel to generate an extraneous output at the 300 MHz IF frequency.

After the BPF the signal is mixed with the voltage controlled local oscillator signal, which is tunable from 1250-1750 MHz and is also controlled by the channel select logic board. This second mixer downconverts the signal to a 300 MHz IF signal which is amplified and then filtered by a 300 MHz bandpass filter with a 30 MHz bandwidth. Due to the tuned performance of this BPF an additional phase equalizer is not required.

The IF output is then amplified by the IF amplifier board which contains two shielded stages of amplification, the first stage of which is controlled by the AGC detector and amplifier.

The amplified IF signal is sent to the Demodulator Board where it is fed into the phase lock loop phase detector and the AGC detector and amplifier. The AGC circuit maintains the phase detector input level at -12 dBm.

The onboard demodulator is a phase locked threshold extension demodulator (Synchronous Receiver). The circuitry is basically simpler than the conventional FM demodulator resulting in lower cost and a more reliable unit. A detailed performance analysis of the phase lock demodulator used in this 12 GHz satellite receiver is presented in Appendix A.

In the phase detector, the input IF signal is compared with the signal from the 300 MHz voltage tuned oscillator. The output of the phase detector is a voltage nominally proportional to the phase difference between the IF and VTO signals. This phase error is amplified by two

separate loops, a low frequency dc phase error loop amplifier, and a high frequency loop containing the second order loop filter and video frequency loop amplifier. The outputs of the two loop amplifiers are summed and applied to the 300 MHz VTO tuning varactor diodes in order to tune the oscillator frequency towards a zero phase error. The summed loop amplifier output is also the demodulated composite video signal which is passed through a de-emphasis network and amplified by the output buffer amplifier. The demodulated composite video signal is then sent to the Signal Processor board where the audio and video signals are separated, filtered, amplified, and sent to the rear panel output ports.

At the Signal Processor board the composite signal is split by a resistive power divider. Half of this signal is fed to the video low pass filter. The low pass filter rejects all signals and noise above its 4.2 MHz cut-off frequency, including the 5.14 MHz audio subcarrier signal. This video signal level is controlled by a 100 Ω potentiometer and is amplified by the video amplifier. Part of the video signal is fed to the sync separater circuit which removes the video sync pulses from the video signal. The sync pulses are then amplified and fed to the clamping diodes, which clamp the video signal to ground during sync time. This clamping action forces a charge on the video coupling capacitor connected to the input of the video output buffer stage such that DC restoration is obtained to the video signal. In addition, this clamping action removes the 30 Hz energy dispersal signal normally present in the satellite system.

The clamped video signal at the output buffer stage is sent to the "F" type Video Output jack on the indoor unit rear panel. The processed video signal is an amplitude adjustable signal nominally 1 volt peak to peak. The polarity of this waveform is black to white positive going.

Going back to the input resistive power divider, the other half of the composite baseband signal is fed to the audio subcarrier demodulator circuit. This signal is fed to a bandpass filter tuned to 5.14 MHz (the audio subcarrier). This filter allows only the subcarrier signal to be fed to the subcarrier demodulator.

The demodulator circuit consist of an on chip limiter, amplifier, FM detector circuit and audio buffer circuit. The output of the buffer circuit is the audio signal resulting from the demodulation produced by the FM detector. This audio signal is applied to the audio level control potentiometer, the 75 microsecond deemphasis circuit and the balanced audio output amplifier. The balanced output audio signal is then routed to the rear panel terminal strip.

The Channel Select Logic/Power Supply board provides the proper control signals for the microstrip tuner to achieve the correct channel selection, and the board also supplies the $\pm$12 volts for the indoor unit circuit functions as well as the unregulated $\pm$20 volts for the outdoor downconverter unit. The channel select logic has been implemented to achieve a low cost and accurate tuning system which automatically compensates for any offsets or temperature drifts in the microstrip UHF VCO or the outdoor unit Gunn LO.

The channel select operation is as follows: The selection of a video channel from the front panel switches triggers a one shot which resets all the logic and counters to the beginning of the sweep mode of operation. At the end of the reset pulse, the logic is activated and the DAC counter begins to count down from its reset value. This decrements the output voltage from the DAC amplifier. This voltage is applied to a voltage shaper whose output voltage follows a non-linear relationship as $V_{OUT} = K\ V_{IN}^{\alpha}$.

The voltage level is then level shifted and applied to tune the UHF VCO on the UHF microstrip tuner. This operation acts to roughly

linearize the sweep of the VCO. Simultaneously, another voltage shaper network is incorporated to apply the proper voltage level to the tunable BPF on the microstrip board. This operation allows the tunable BPF and UHF VCO to track each other.

As the VCO sweeps, a sampled output is supplied to the sampler circuit on the Demodulator board. The VCO sample is mixed with a harmonic of a 40 MHz signal generated by a 40 MHz oscillator and step recovery diode. When the VCO frequency approaches a harmonic of the 40 MHz signal a pulse is sent out of the sampler circuit. This pulse is amplified and sent to the pulse counter on the channel select logic board. As the VCO sweeps, pulses will appear at the sampler output. Since the VCO sweeps down from 1750 to 1250 MHz and because the VCO sample is low pass filtered for frequencies below 1740 MHz, the first output pulse from the sampler, during the sweep mode of operation, corresponds to a UHF VCO frequency of 1720 MHz, the 43rd harmonic of 40 MHz, and the tuner condition for reception of the 12th channel in the RF band at 12.17 GHz. For selection of the 1st channel in the RF band at 11.73 GHz, twelve sample pulses must be counted, thereby tuning the UHF VCO to 1280 MHz.

For this contractual development program, the outdoor downconverter was specified for operation with an LO at 10.75 GHz, and the RF transmitter frequency was specified at 12080.5 MHz. With the tuning scheme incorporated in this receiver, reception of this RF carrier will be on channel 10. Note that for the above specified LO and RF frequencies the resultant downconverted frequency is 1330 MHz which is 10 MHz greater than the specified 1340 MHz input frequency to the demodulator unit for reception of channel 10. This offset frequency is nulled out by sensing the demodulator phase detector error which forces the DAC to up/down count to null out the dc phase error automatically, thus ensuring optimum video reception. This 10 MHz offset in the IF frequency is well within the capture range of the automatic fine tuning circuitry. For future units using the 12080 MHz RF carrier, we will request that the

downconverter LO be specified at 10.74 GHz. With the present LO and RF frequencies assigned to the downconverter unit, no degradation in the signal reception will result.

The channel select logic also provides one other control function. The sensing of the video sync pulses from the signal processor board allows the control logic to respond to the dc phase detector error only when video is present. When video is not present at the channel selected, the tuner will not respond to any erroneous signals that may possibly be present in the frequency band selected.

1.2 RECEIVER PERFORMANCE DATA SUMMARY

The performance of this satellite receiver is described in the following table giving both the specifications and nominal performance results. The measurement procedure is described in the acceptance test plan listed in Appendix B. The test procedure is divided into two main sections. First, the Downconverter Unit is tested to measure its electrical performance. Then, the Downconverter and Demodulator Units are tested together to prove conformance with the RF, video, and audio specifications. Table 1-1 lists the receiver specifications and performance data summary. The present prototype downconverter unit has an excessive weight of 5.5 lbs. (2.5 kg). This is because of the use of brass rather than aluminum for the FET amplifier module and excessive aluminum bulk in the downconverter chassis. The downconverter weight can be reduced well below 5.0 lbs (2.25 kg) by using all aluminum chassis and minimizing extraneous aluminum bulk. In all other areas, the prototype receiver meets or exceeds the specifications.

The test results were obtained for an RF carrier at 12080 MHz. Through the downconverter is designed for operation in the complete frequency band from 11.7 to 12.2 GHz, the present prototype achieves a degraded noise figure above and below 12080 MHz. This is due to a less than optimum downconverter design and is easily optimized for future units. This design will be further explained in Section 2.2.

TABLE 1-1

12 GHz SATELLITE VIDEO RECEIVER SPECIFICATIONS

SPECIFICATIONS	
Outdoor Unit	
Input Frequency Range	11.7-12.2 GHz
Input Connector	WR-75 Cover Flange
Input Level	-72 to -87 dBm
Input Return Loss (VSWR)	10 dB minimum (2:1 max)
Output Frequency Range	0.950 GHz to 1.450 GHz
Output Connector	Type "F", Female
Input DC Power	+20 VDC at 240 mA maximum -20 VDC at 180 mA maximum
Operating Temperature Environment	-35°C to +50°C
Operating Humidity Environment	0-100% Relative Humidity
Weight	<5.0 lbs. (2.5 kg.)
Indoor Unit	
Input Frequency Range	0.950 GHz to 1.45 GHz
Input Level	-55 to -25 dBm
Input Connector	Type "F", Female
Video Output Connector	Type "F", Female
Video Output Impedance	75 Ω
Video Output Return Loss	15 dB minimum
Video Output Level	1 V peak-to-peak (adjustable)
Video Polarity	Black to white, positive going
Audio Output Connector	Screw Type terminal strip
Audio Output Impedance	600 Ω, balanced
Audio Output Level	0 dBm (adjustable)
Audio Subcarrier Frequency	5.14 MHz
AC Power Requirements	115V ±10% at 25 watts maximum
Operating Temperature Environment	+10°C to +40°C

TABLE 1-1 (CONTINUED)

12 GHz SATELLITE VIDEO RECEIVER SPECIFICATIONS

Description	Specification (@ 24°C)	Test Results			
Outdoor Unit Temperature	24°C	24°C	-35°C	+50°C	+50°C
Indoor Unit Temperature	24°C	24°C	0°C	+50°C	0°C
Downconverter Tests					
Downconverter Gain	52 ±6 dB (at 12080 MHz)	49.4 dB	51.6 dB	47.1 dB	47.1 dB
Local Osc. Stability	10750 ±4 MHz	10747.4 MHz	10746.4 MHz	10746.4 MHz	10746.4 MHz
RF Input VSWR	2:1 max	1.2:1	*	*	*
Image rejection	15 dB min	>740 dB	*	*	*
Receiver NF	4 dB max	3.95 dB	3.25 dB	4.60 dB	4.60 dB
Demodulator RF Tests					
Static Threshold	C/N_i < 8 dB	6.5 dB	**	**	**
Signal-to-Noise, Weighted at C/N = 12 dB	48.5 dB min	49.0 dB	**	**	**
Dynamic Threshold	C/N_i < 11 dB	10.5 dB	9.75 dB	11.5 dB	11.5 dB
Signal-to-Hum Ratio	50 dB min	50 dB	50 dB	50 dB	50 dB
Video Baseband Parameters					
Gain Frequency Distortion	50 ±3 IRE	50^{+0}_{-3}	50^{+0}_{-3}	50^{+0}_{-3}	50^{+0}_{-3}
Field Time Distortion	±2 IRE	+2, -0	+2, -0	+2, -0	+2, -0
Line Time Distortion	±2 IRE	+2, -0	+2, -0	+2, -0	+2, -0
Short Time Distortion	100 ±6 IRE	100 IRE	100 IRE	100 IRE	100 IRE
Impedance Level and Return Loss	70 ±10 IRE	72 IRE	72 IRE	72 IRE	72 IRE
Differential Gain	2%	2%	2%	2%	2%
Differential Phase	1 Degree	1°	1°	1°	1°
Chrominance-Luminance Gain	100 ±3 IRE	101 IRE	101 IRE	101 IRE	101 IRE
Chrominance-Luminance Delay	50 ns	<10 nsec	<10 nsec	<10 nsec	<10 nsec
Audio Baseband Parameters					
Output Impedance and Return Loss	6 dB ±1.4 dB	5.8 dB	5.8 dB	5.8 dB	5.8 dB
Frequency Response Flatness	30 Hz-15 KHz, 3 dB 100 Hz-10 KHz, 1 dB	1.75 dB 0.25 dB	1.85 dB 0.25 dB	1.8 dB 0.3 dB	1.75 dB 0.25 dB
Distortion	5% max	0.55%	0.75%	1.1%	0.6%
Test Tone Signal-to-Noise	45 dB min	47 dB	46 dB	45 dB	47.5 dB
Static Threshold	C/N_i < 10 dB	9.6 dB	9.0 dB	10 dB	9 dB

*Because 24°C test results were well within the specification limit, these tests were not performed over temperature. No degradation from room temperature is expected.

**Not measured due to the test requirements to measure the static threshold (as explained in the test plan Appendix B). Performance expected to follow the measured dynamic threshold.

1.3 PROJECTED RECEIVER NOISE FIGURE PERFORMANCE OVER PRODUCTION

With the objective to develop 12 GHz receivers at low cost with noise figures of 4 dB or less, the key element in our receiver front end (outdoor unit) is a low noise FET amplifier, and the most important cost consideration is in the FET devices.

The receiver front end design is based on a low noise three stage FET amplifier utilizing 0.5 μm gate length GaAs FET devices. The design concept is to capitalize on a fast maturing technology to allow design margin for the rest of the receiver necessary for low cost production. Another important consideration is to achieve high receiver performance based on a modern technology, such that the receiver will be compatible with the rapidly advancing satellite communication technology for many years to come, and not to become obsolete because of the continuing advancement in FET device performance.

The FET amplifier is assembled from three separate stages which are independently evaluated and tuned for gain and noise figure. Since the major contribution to the receiver noise figure is from the FET amplifier, the input amplifier stage is specifically screened to consistently yield the lowest noise figures. This selection process will tend to limit the variation of the receiver noise figure from unit to unit during the production phase.

The projected gain and noise figure distributions, based on our FET amplifier, bandpass filter, mixer and IF amplifier designs are tabulated in Table 1-2. This distribution shows that the expected nominal noise figure performance at 24°C meets or exceeds the 4.0 dB specifications. Since the FET performance degrades at higher temperatures, the worst case performance at 50°C is projected to be 4.34 dB.

TABLE 1-2

RECEIVER FRONT END PROJECTED GAIN AND NOISE FIGURE PERFORMANCE OVER PRODUCTION

	Nominal +24°C		Worst Case +24°C		Worst Case +50°C	
Component	Gain (Loss)	NF	Gain (Loss)	NF	Gain (Loss)	NF
1. Input Loss	(0.2 dB)	0.2 dB	(0.2 dB)	0.2 dB	(0.2 dB)	0.2 dB
2. FET Amplifier	21.5 dB	3.4 dB	21.0 dB	3.6 dB	19.5 dB	3.8 dB
3. Band Pass Filter	(1.5 dB)	1.5 dB	(1.5 dB)	1.5 dB	(1.5 dB)	1.5 dB
4. Mixer	(6.0 dB)	6.0 dB	(7.0 dB)	7.0 dB	(7.0 dB)	7.0 dB
5. IF Post Amplifier	4.2 dB	4.0 dB	39.0 dB	4.5 dB	39.0 dB	4.5 dB
Total Receiver	55.8 dB	3.78 dB	51.2 dB	4.06 dB	49.7 dB	4.34 dB

$NF_{receiver} = 10 \log F_R$

where

$$F_R = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \frac{F_5 - 1}{G_1 G_2 G_3 G_4}$$

and F_i, G_i refers to the noise figure (ratio) and gain (ratio) for i th component listed above.

This distribution is based on the use of a device similar to the NEC 38800 GaAs FET (Nippon Electric Company) currently used in our amplifier. This device's performance was used for bugetary purposes since a production device of comparable performance is projected to be much less in cost in the following years. Indeed, it is Hughes' aim to make this production device available at $30/chip device in 1000 lot quantities in two years' time.

Hughes projected FET amplifier costs are discussed further in Section 4.0.

2.0 OUTDOOR DOWNCONVERTER UNIT DESCRIPTION AND PERFORMANCE

2.1 GENERAL

The outdoor downconverter unit translates the input RF signal to an IF frequency between 950 and 1450 MHz. The unit is specified for operation in the 11.7-12.2 GHz band for an input power level between -72 dBm and -87 dBm.

This downconverter for the 12 GHz receiver is housed in a cylindrical can 128.3 mm (5.05 inches) in diameter times 173.7 mm (6.84 inches) in length with a weight under 2.268 kg (5.0 pounds). The unit has been designed to be conveniently mounted on the waveguide feed of the receiver antenna. The unit is weatherproof for 0-100 percent relative humidity and specified for outdoor operation over the temperature range -35°C to +50°C.

The assembly drawing for the outdoor unit is shown in Figure 2-1. All RF and power connectors are located on the 160 mm (6.30-inch) diameter cover. The waveguide flange feeds directly into the input isolator. J1 is a four pin weatherproof connector which is the receptacle for the 100 foot power cable coming from the indoor unit which sends the ±20 volt unregulated power, the power return, and the signal strength indicator voltage. J2 is the type "F" receptacle for the 100 foot long coaxial cable which transmits the Downconverter IF output to the indoor unit. This inexpensive cable has a nominal 13 dB loss per 100 feet for the 950-1450 MHz IF signal. TP2 is the test point for monitoring the signal strength level. The voltage level at this monitor point is observed and minimized when pointing the receive antenna. This insures maximum RF signal reception. TP1 is the ground reference test point.

The outdoor unit chassis serves as the mounting structure for the various outdoor unit subassemblies, which are the low noise FET amplifier and BPF subassembly, the mixer subassembly, the Gunn diode local oscillator

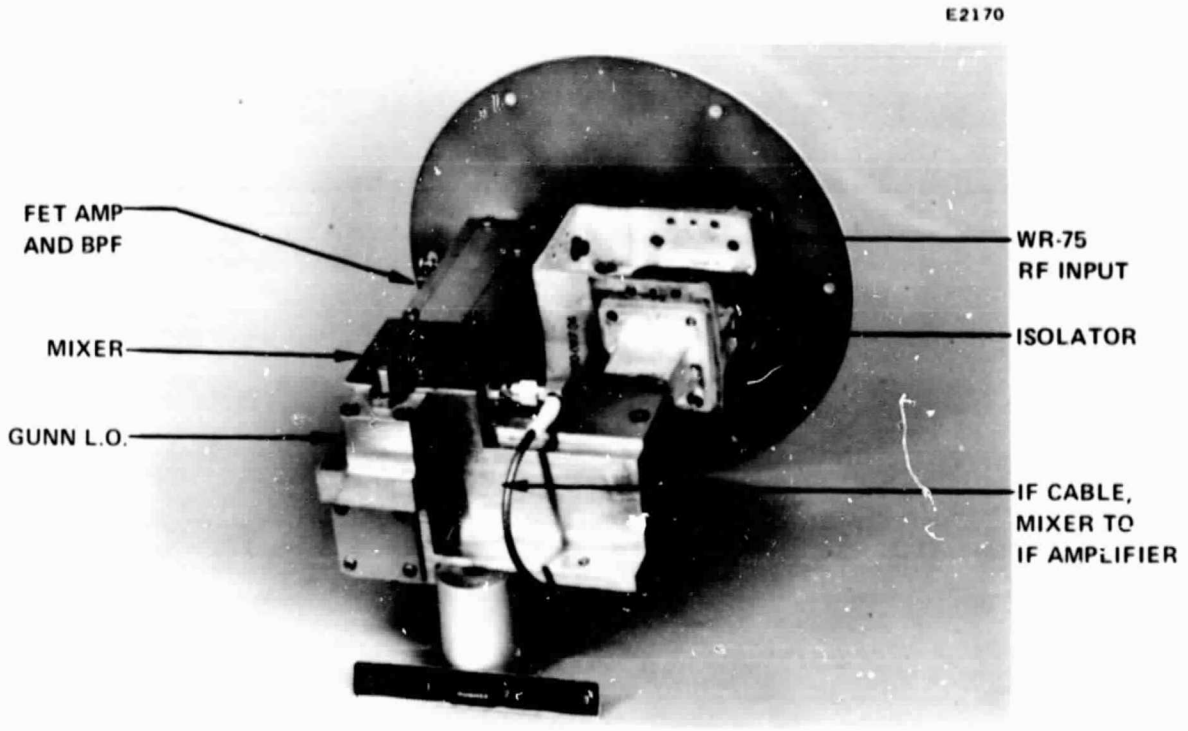

Figure 2-1A Outdoor downconverter, final assembly.

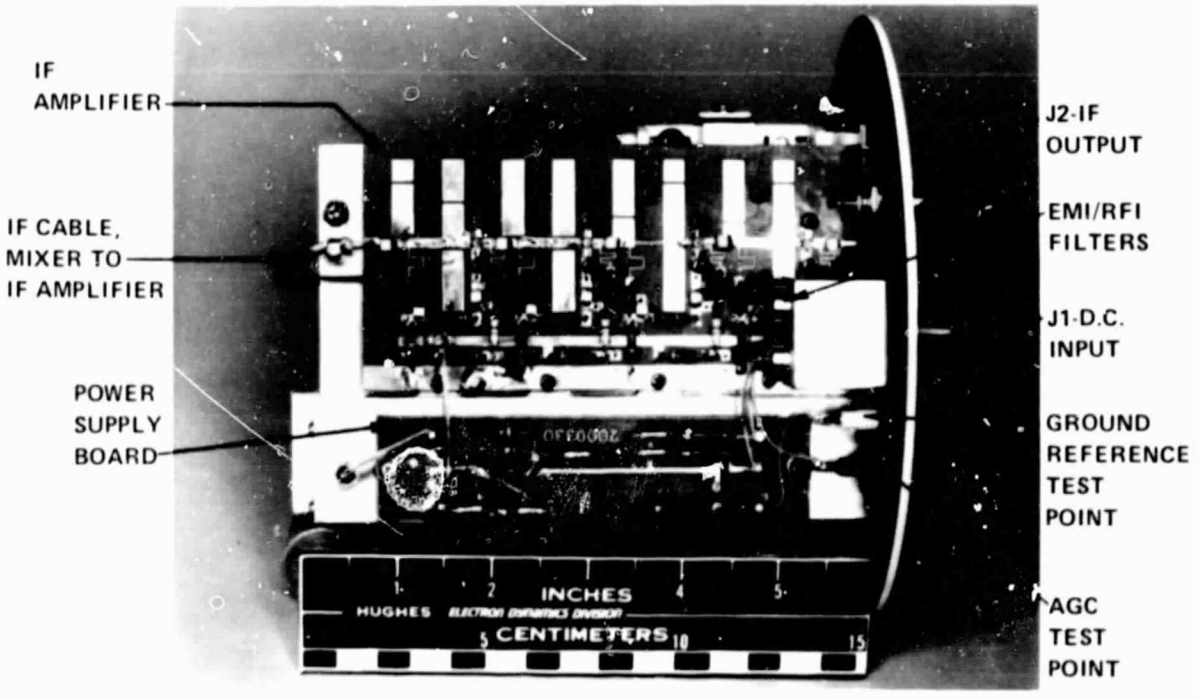

Figure 2-1B Outdoor downconverter, final assembly.

subassembly, the IF amplifier subassembly, the power supply board subassembly. The description and performance of each of these subassemblies is presented individually.

2.2 FET AMPLIFIER AND BAND PASS FILTER SUBASSEMBLY

The three stage low noise FET amplifier and the three section Chebychef band pass filter are contained in the same housing. The waveguide isolator is attached to this subassembly before mounting on the outdoor unit chassis.

The prototype unit does not contain any internal isolators and was tuned specifically for operation at 12080 MHz. Being the preliminary design of the FET module, this prototype has a gain and noise figure response that is quite sensitive to output loading conditions and has resulted in degraded performance at frequencies above and below 12080 MHz. Its gain and noise figure response are shown in Figure 2-2. The noise figure shown is the total downconverter noise figure with the mixer and IF amplifier at the FET module output.

Because of this preliminary design, the prototype FET module's characteristics are less than optimum. Due to time limitations, an improved FET module design presently in development was not included in the prototype. This new design will yield a passband response with a nominal gain of +20 dB ±0.25 dB and a nominal noise figure below 4.0 dB across the entire frequency band from 11.7 GHz to 12.2 GHz. This will be achieved by supplying internal isolators to the FET module to result in better interstage matching and low sensitivity to output load mismatches. Since this unit is intended for use in the future downconverter units, the following discussion will pertain to the FET module with the internal isolators.

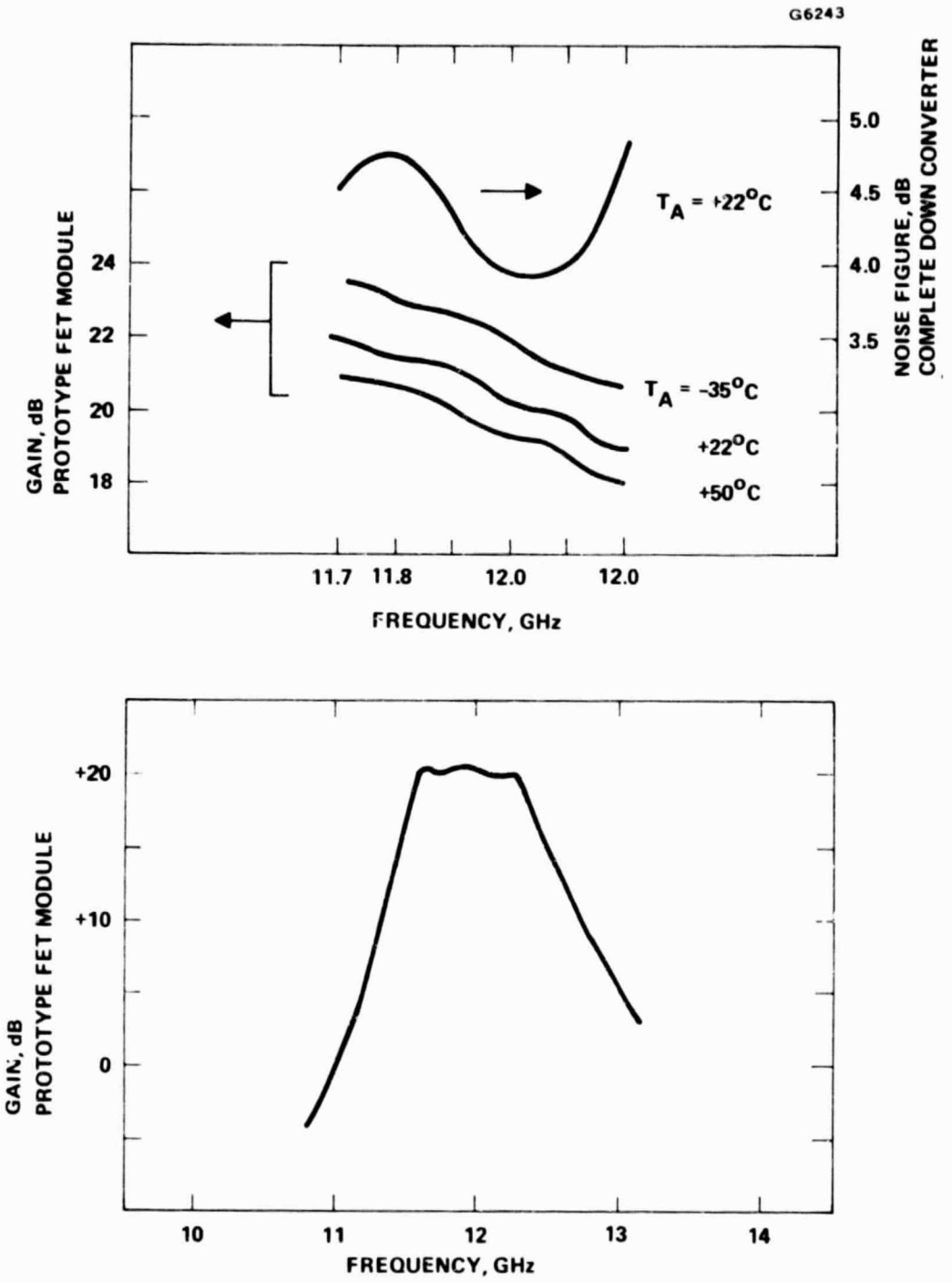

Figure 2-2 FET amplifier subassembly, gain and noise figure response (for amplifier without internal isolators).

Figure 2-3 shows the low noise FET amplifier module (LNA) and is a three stage FET amplifier with bandpass filter and two internal isolators. The first isolator, between the second and third amplifier stages, minimizes interstage mismatch effects and allows independent amplifier tuning. The second isolator results in a bandpass response which is insensitive to load mismatches. All internal modules are constructed using thin film MIC technology on alumina or garnet substrates. The LNA is a self contained, hermetically sealed unit which will achieve reliable performance over the extremes of its outdoor environment.

Each component in the LNA has its own carrier to facilitate assembly and test of the individual modules. The carriers for the amplifier stages and filter are Kovar to match the expansion coefficient of the alumina substrates. The MIC isolators use molybdenum carriers to match garnet expansion and because of molybdenum's anti-magnetic characteristic.

All carriers are soft-gold plated, and all substrates are gold sputtered. All assembly is done with fluxless gold alloy soldering and all connections are gold wire or gold ribbon.

The MIC filter is etched from a chromium/gold metallized alumina substrate using standard photolithographic techniques. The substrate is then soldered to its Kovar carrier using gold/tin alloy solder at 280°C.

The amplifier substrates are alumina metallized with tantalum nitride/molybdenum/gold. The tantatum nitride is used as thin film resistors for the FET bias circuits. The circuits are defined and etched with standard techniques, except they must be etched a second time to define the resistor patterns. The substrates are then heat-treated above 450°C to stabilize the tantalum nitride resistors. D.C. blocking capacitors are soldered to the substrate at 400°C using gold/silicon alloy solder. The substrates and RF bypass capacitors are next soldered to the Kovar carriers using gold/germanium alloy solder. Circuit

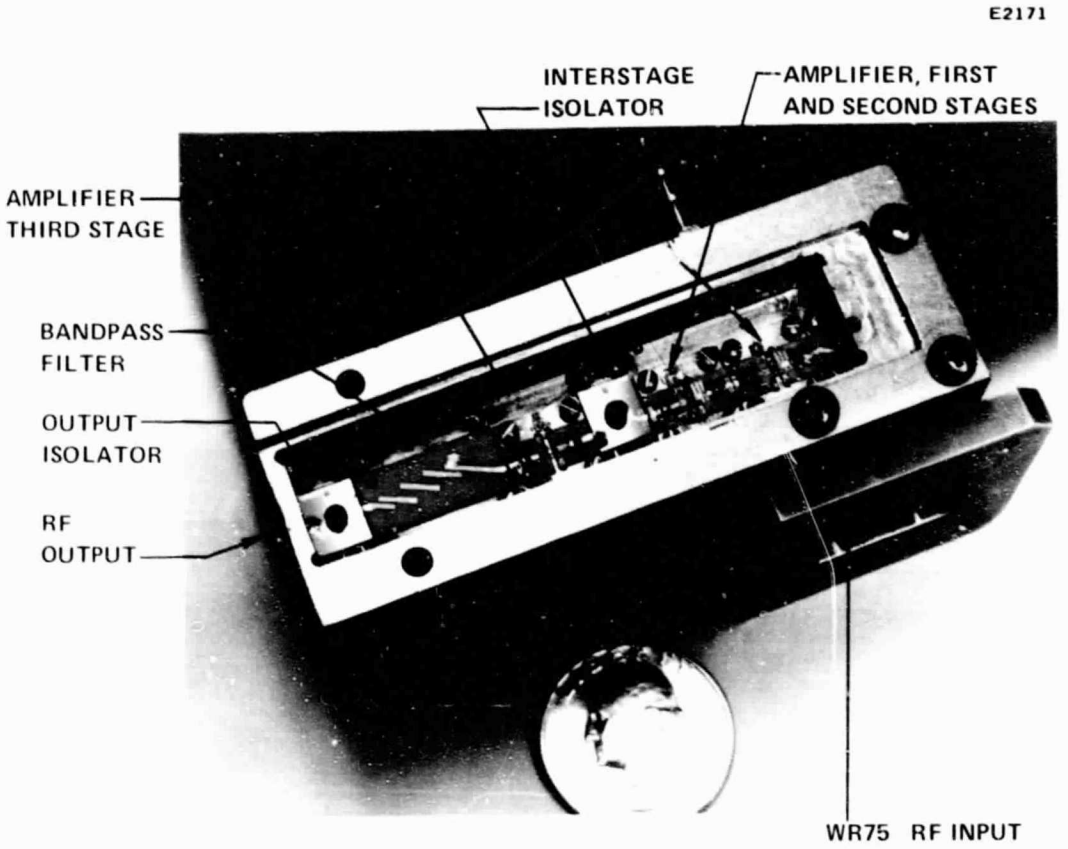

Figure 2-3 FET amplifier and BPF, assembly.

interconnects are now bonded before the FET is installed to prevent damage to the FET. The final assembly step is to attach the FET and source bypass capacitors to the carrier using gold/tin alloy. The FET is then finally wire bonded into the finished circuit. The single stage modules are placed in test fixtures and tuned for best noise figure.

The MIC isolators are etched from chromium/gold metallized calcium vanadium garnet substrates. A 50 ohm chip resistor is soldered to the garnet substrate using gold/germanium alloy and this assembly is then soldered to a molybdenum carrier using gold/tin solder. The final assembly step is the connection of the ground pad on the garnet substrate to the carrier. This is accomplished with a wide gold ribbon that is gap-welded to the substrate and carrier. The completed isolator is installed in a test fixture and the appropriate samarium-cobalt biasing magnets are selected. The magnets are attached using a low-loss epoxy.

The individual components are then mounted in the LNA housing using 0-80 screws. The housing is aluminum with nickel and gold plating. Hermetic RF and DC feed throughs are soldered in the housing using lead/tin/silver solder. The modules are interconnected, and connected to the housing connectors, with gold ribbon that is gap-welded. The housing is hermetically sealed using moisture resistant film adhesive in a nitrogen atmosphere after a two hour bake-out.

The inclusion of the internal isolators to the FET module assembly will not increase the cost of this assembly. Though these extra components will increase the parts cost, their use will relax the tuning and testing constraints on the individual FET amplifier stages and on the complete assembly. Thus, labor costs are expected to decrease to offset the added parts cost.

2.3 MIXER SUBASSEMBLY

The mixer is a branchline coupled balanced mixer etched on 0.38 mm (0.015 in.) thick Duroid substrate material. This subassembly is shown in Figure 2-4. The mixer diodes are high cutoff frequency silicon Schottky beam lead diodes specifically designed for the X-Band use. The mixer design consists of a 90°, 3 dB hybrid junction (labeled a), quarter wavelength shorted stubs (labeled b), quarter wavelength open circuited stubs (labeled c), and two beam lead mixer diodes bridging the two circuit gaps at d. The 90°-hybrid affords a good match at the LO and RF ports and is a two section junction to achieve wide bandwidth performance. The shorted quarter wavelength stubs provide d.c. return for the mixer diodes and appear as an RF choke for the 12 GHz signal. The open circuited quarter wavelength stubs reject the RF signals at the IF output port. The typical conversion loss of this mixer as a function of RF frequency with an LO at 10.75 GHz is 6 dB ±0.5 dB at 11.7 to 12.2 GHz.

2.4 GUNN LOCAL OSCILLATOR SUBASSEMBLY

The local oscillator is a cavity stabilized Gunn diode oscillator operating at 10.75 GHz $\pm$4 MHz with a nominal output power of 30 mw. The stability of the oscillator is specified over the temperature range of -35°C to +50°C. The Gunn diode is mounted on a copper heat sink with bias supplied through a 0.33 mm diameter hole in the base plate. The cavity housing is made of aluminum whereas the tuning post is made of invar. This oscillator is a re-entrant coaxial cavity Gunn oscillator. The cavities radius is large compared to the cavity length and the oscillator operates in a radial transmission line mode similar to the TM010 mode of a circular cavity. The oscillator assembly is shown in Figure 2-5. This combination of materials, used in the oscillator housing, with their different coefficients of thermal expansion, interact so as to provide a temperature compensation mechanism cancelling the diode's inherent tendency to shift in frequency response over temperature.

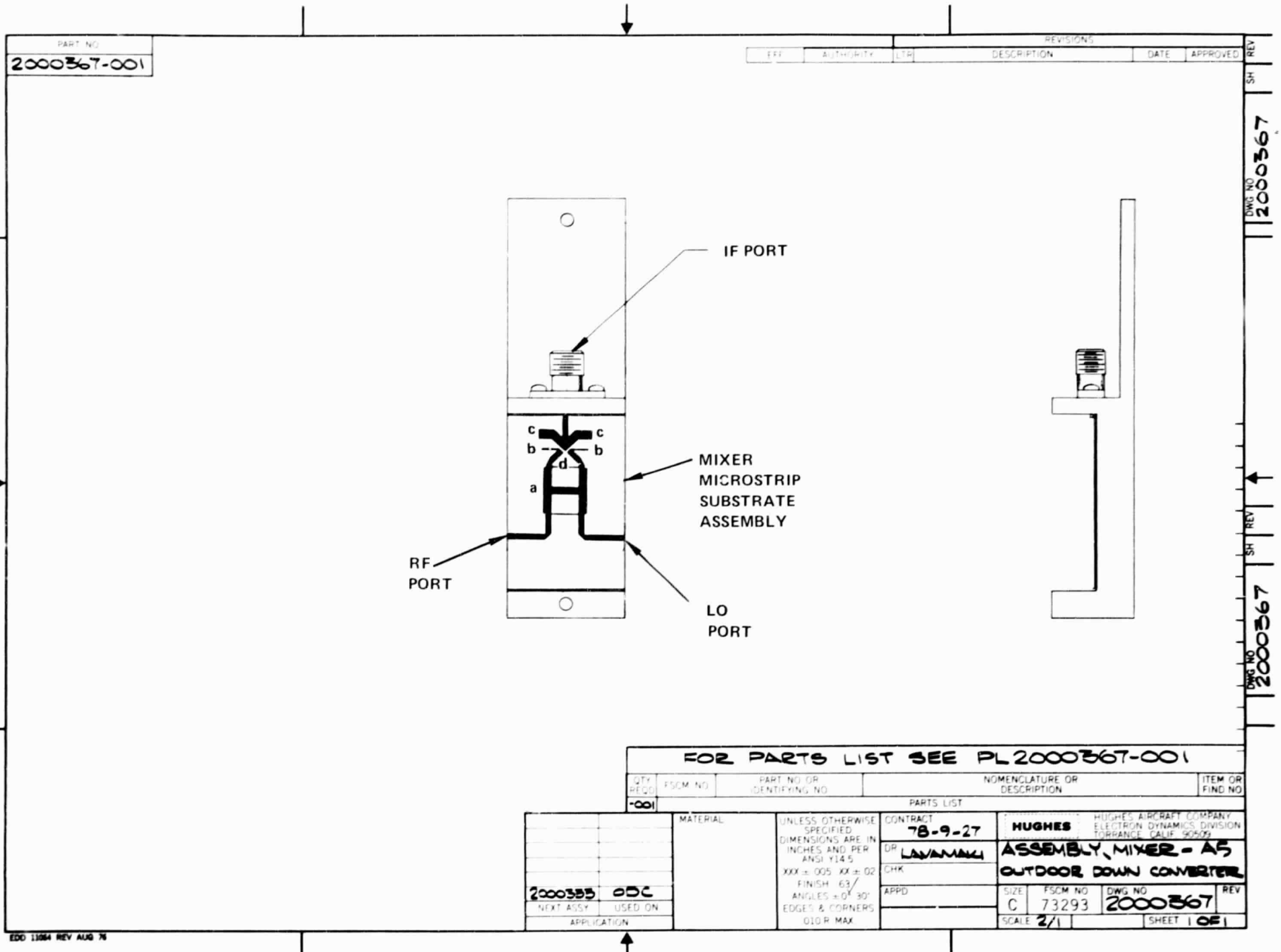

Figure 2-4 Mixer, assembly.

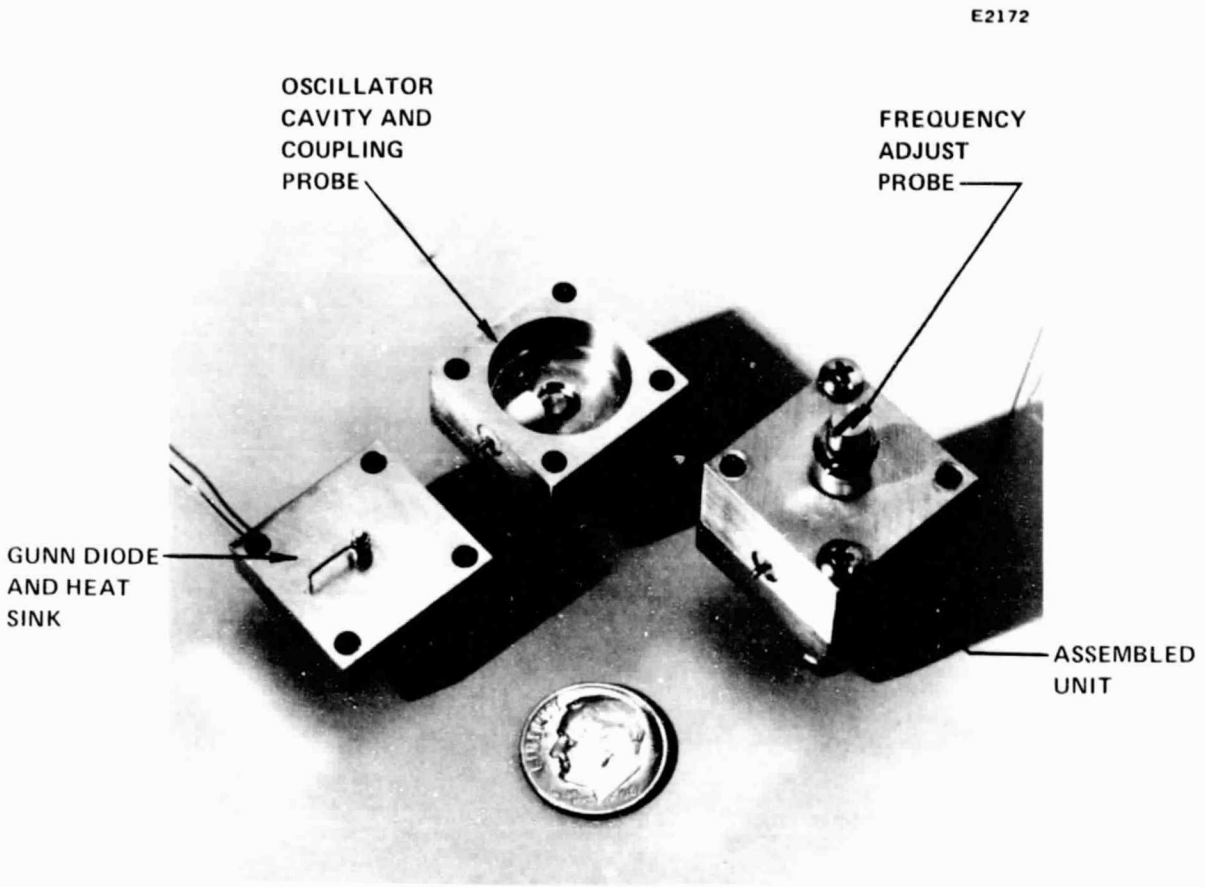

Figure 2-5 Gunn oscillator, assembly.

Figure 2-6 shows the nominal oscillator output frequency and power as a function of temperature. As the figure shows, frequency stability is less than ± 4 MHz over -35 to +50°C. The power supplied to the oscillator is nominally 160 ma from the negative voltage regulated supply.

2.5 IF AMPLIFIER SUBASSEMBLY

The IF Amplifier is a four stage bipolar transistor amplifier with a nominal 42 dB gain and 4.0 dB noise figure over the IF frequency range of 950 to 1450 MHz. The amplifier input is from the mixer IF output, and the amplifier output is connected to the output type "F" connector J2. The IF amplifier schematic is shown in Figure 2-7 and the assembly is shown in Figure 2-8. Each amplifier consists of microstrip input and output matching stages and dc biasing network.

Figure 2-9 shows the amplifier noise figure and gain response over temperature from -35°C to +50°C. As the figure shows, variation over temperature is less than ±0.5 for each parameter. The power supplied to this unit is +12 volts at 160 ma.

2.6 POWER SUPPLY SUBASSEMBLY

The power supply subassembly regulates the input unregulated ±20 volts to supply +12 volts, +6 volts, and -7.5 volts for the other outdoor unit subassemblies. The unregulated voltage input from J1 is first filtered for EMI/RFI before entering the outdoor unit interior and sent to the power supply board. The power supply schematic is shown in Figure 2-10 and the assembly is shown in Figure 2-11.

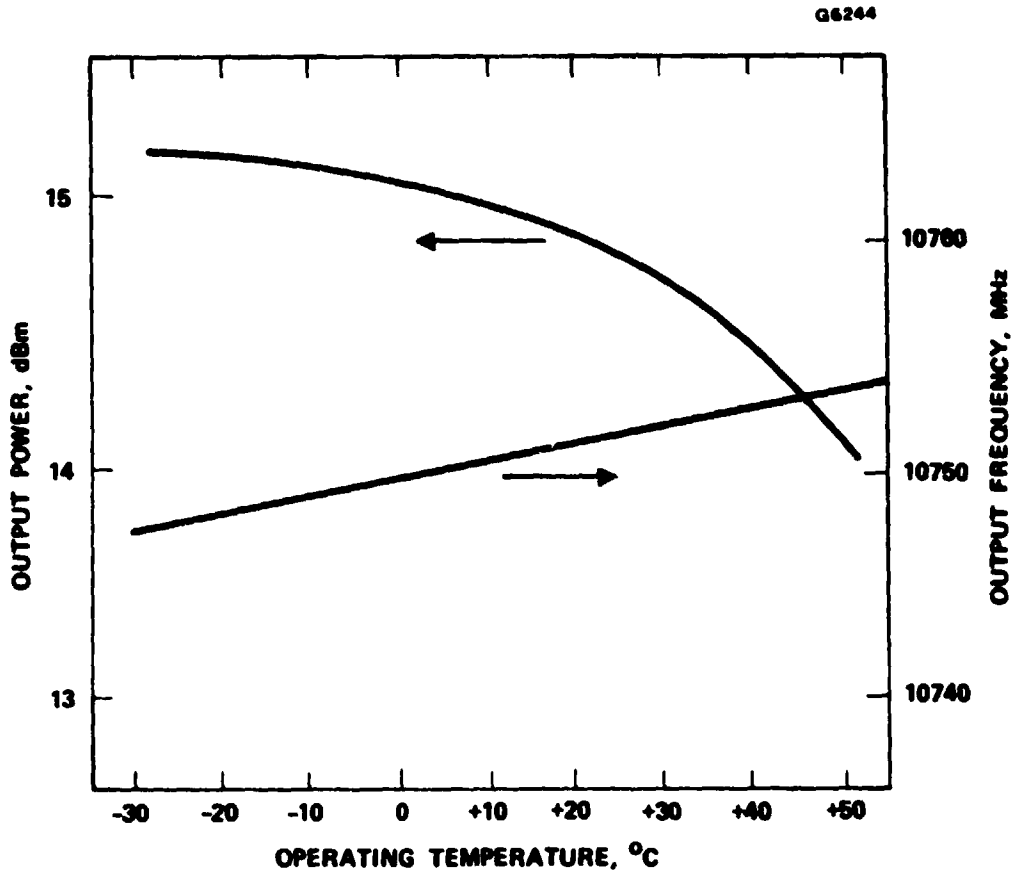

Figure 2-6 Gunn oscillator, output frequency and power as a function of temperature.

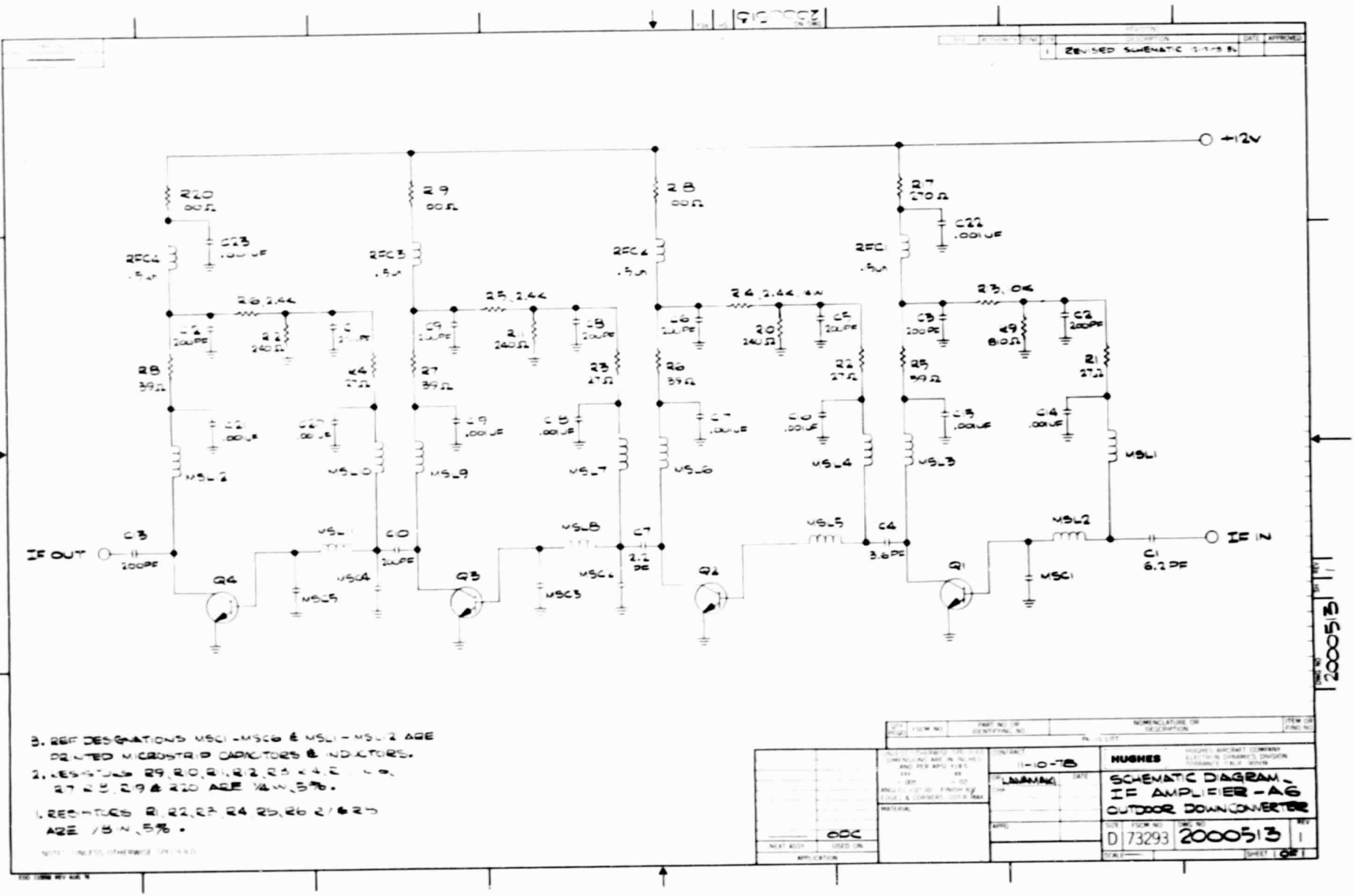

Figure 2-7 Outdoor IF amplifier, schematic.

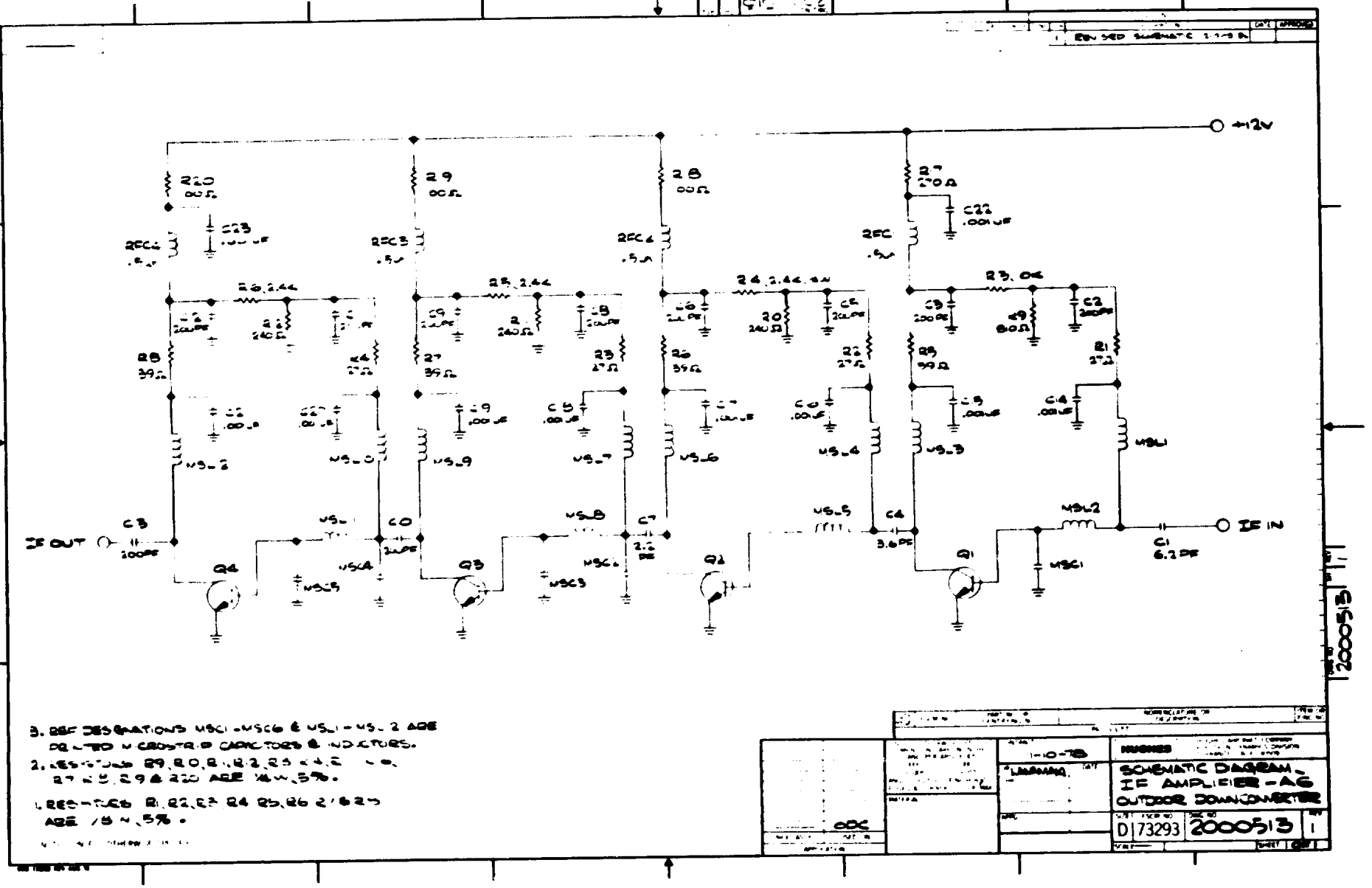

Figure 2-7 Outdoor IF amplifier, schematic.

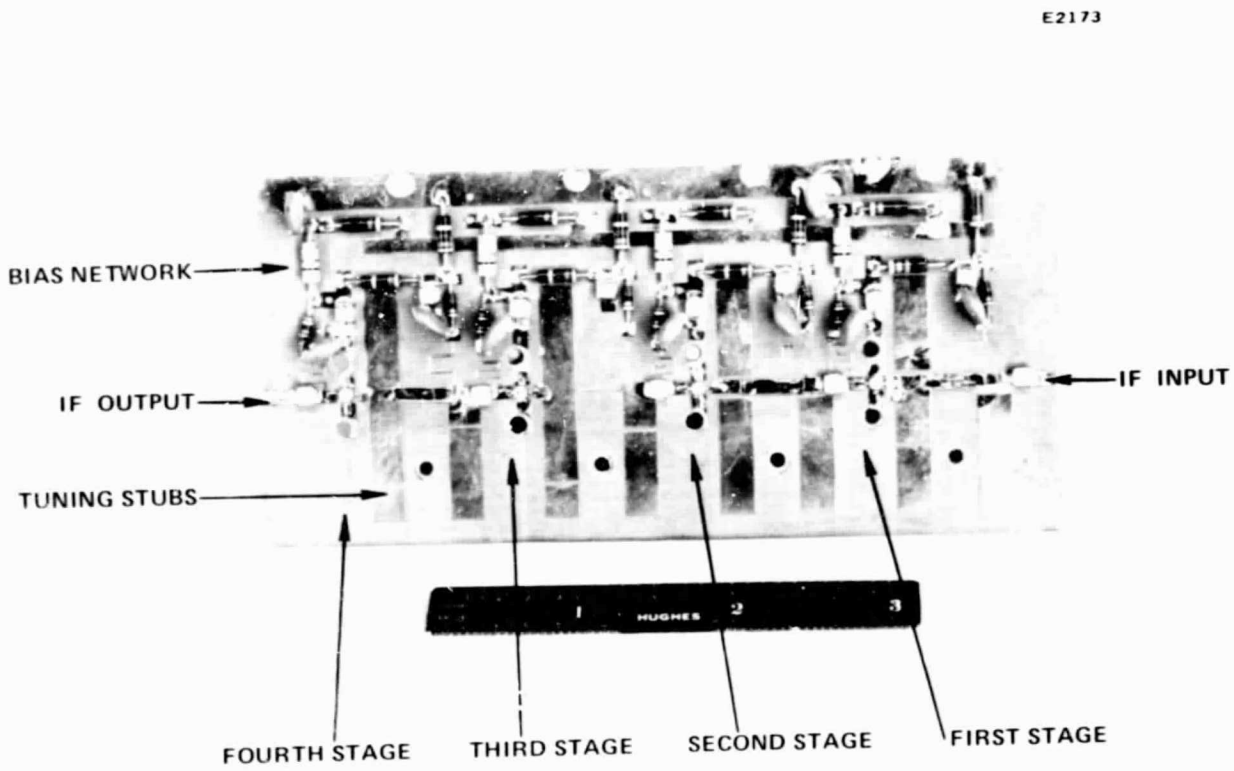

Figure 2-8 Outdoor IF amplifier, assembly.

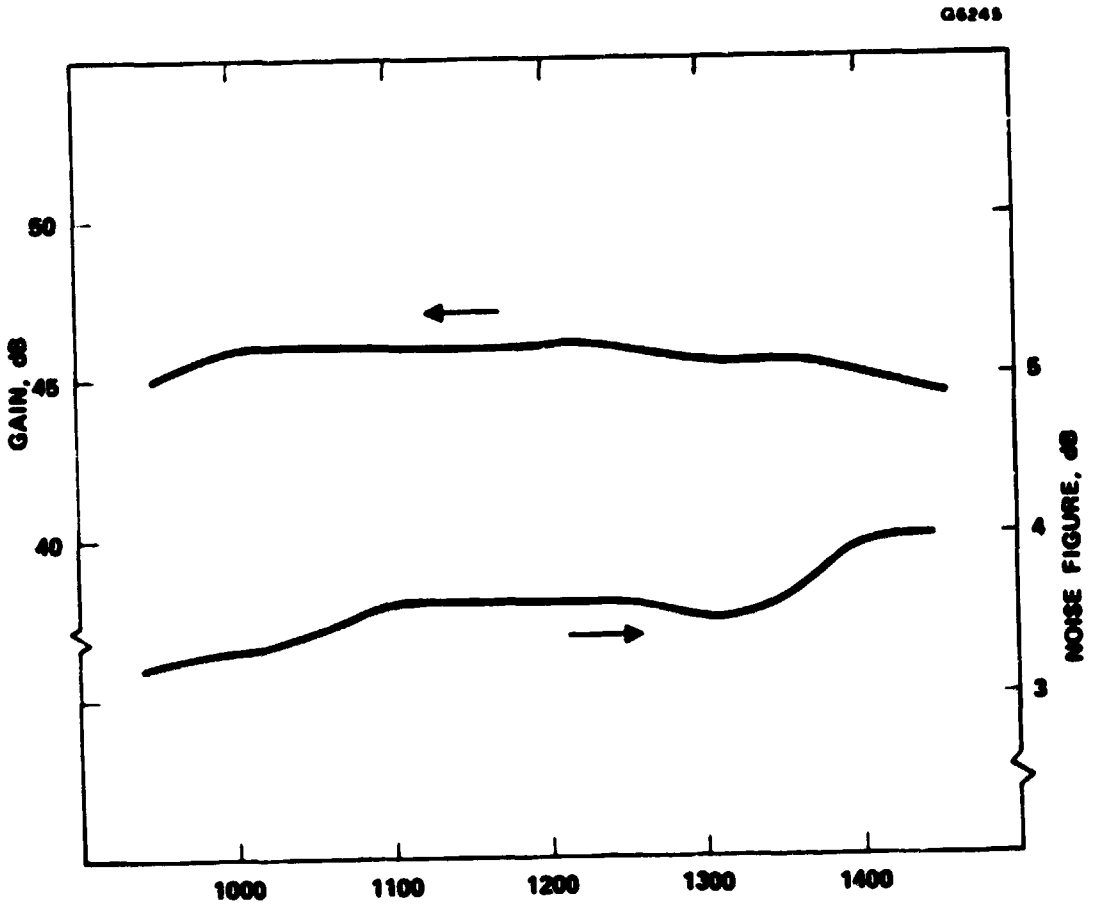

Figure 2-9 Outdoor IF amplifier, noise figure and gain response.

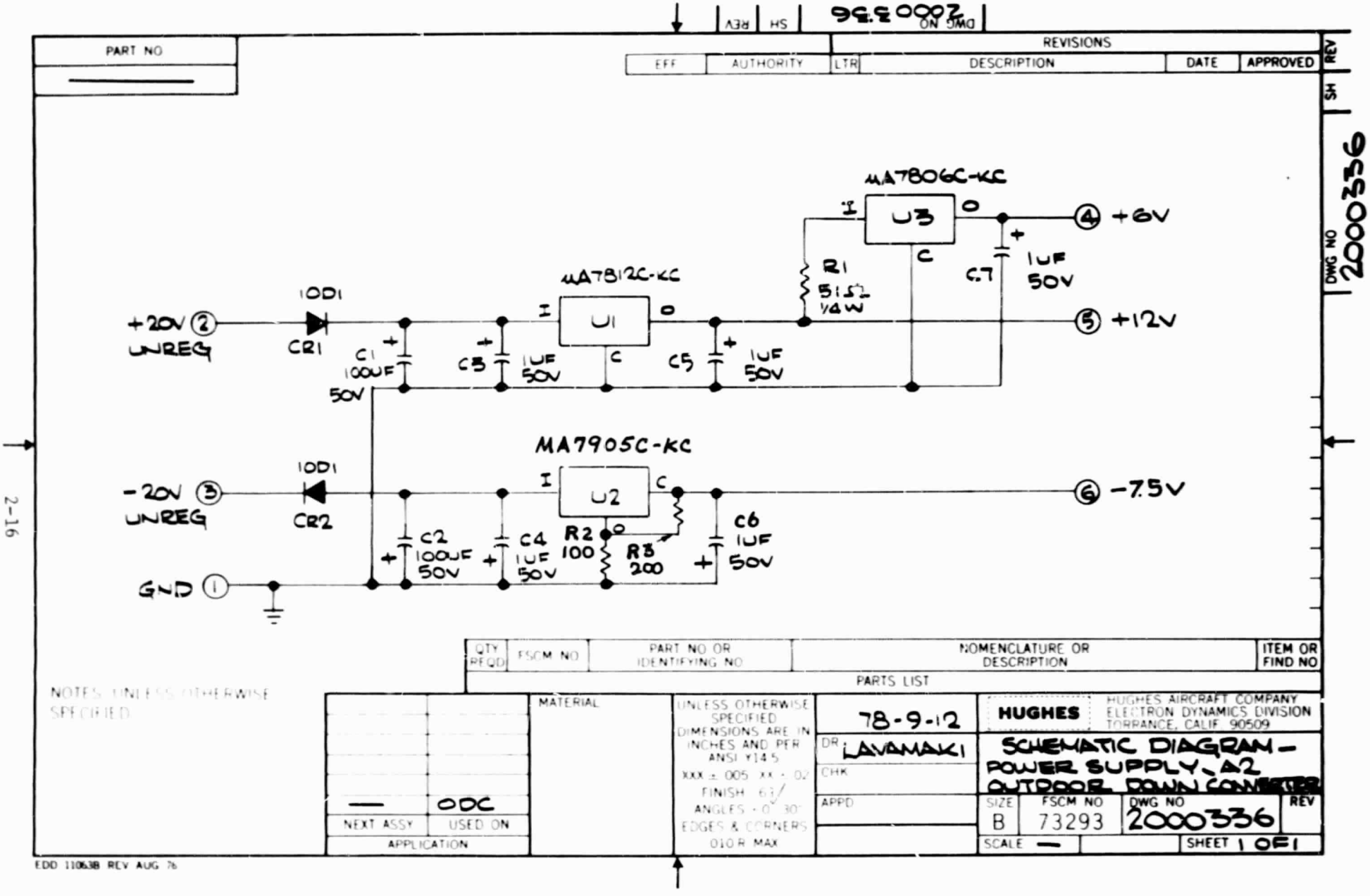

Figure 2-10 Power supply board, schematic.

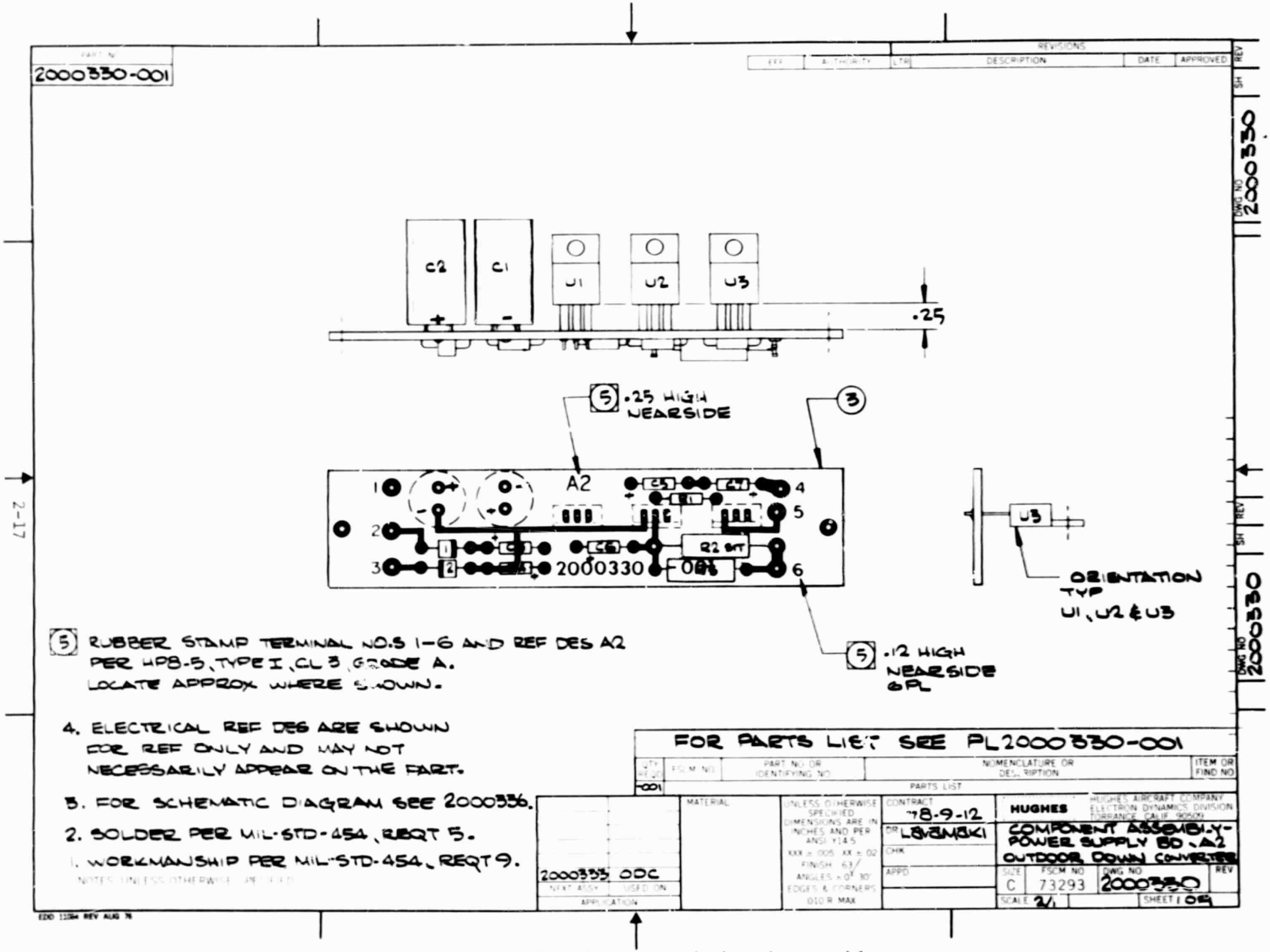

Figure 2-11 Power supply board, assembly.

2.7 TEST AND EVALUATION

For maintaining reliable performance on a production basis and to facilitate ease of field and laboratory repair, the subassemblies comprising the outdoor unit must be interchangeable. To minimize required system testing and to minimize fault location time, each subassembly will be tested and aligned. Their performance parameters must fall within specified tolerances to pass Go/No Go functional tests.

For the five subassemblies in the outdoor unit, the functional tests with specified tolerances are listed in Table 2-1. These tests are designed to reject the out of specification units. In order to save cost, only essential testing relevant to the key performance parameters is carried out. The rejected units will be inspected at a control point to determine whether a specific unit will be reworked or scrapped. The accepted subassemblies will be integrated in the chassis to form a complete outdoor unit. The complete unit will be tested in terms of noise figure, IF bandwidth, gain ripple, RF to IF gain, image rejection, and input VSWR following the test procedure in Appendix B. These tests can be automated by a special console designed specifically for these tests.

The estimated time to complete the final test of the complete outdoor unit chassis assembly is 0.5 hour per unit for 1000 unit production.

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TABLE 2-1

OUTDOOR UNIT SUBASSEMBLY FUNCTIONAL TESTS

Subassembly	Test	Acceptance Specification
FET Amplifier and BFP	Noise figure	<3.6 dB, 11.7-12.2 GHz
	Gain	>19.5 dB, 11.7-12.2 GHz
	3 dB Bandwidth	11.5 to 12.4 GHz minimum
	Gain ripple	<±0.25 dB, 11.7-12.2 GHz
	Input return loss	>10 dB
	Output return loss	>10 dB
	DC Power input	<80 ma at 6 volts
Mixer	Conversion loss	<6.5 dB, 11.7-12.2 GHz RF input
	RF return loss	>10 dB
	LO return loss	>10 dB
	IF return loss	>10 dB
Gunn Local Oscillator	Operating frequency	10.75 GHz ±4.0 MHz
	Output power	>20 mW
	Output return loss	>10 dB
	DC Power input	<180 ma, bias voltage is between -6 and -12 V dependent on Gunn diode.
IF Post Amplifier	Gain	>39 dB, 11.7-12.2 GHz
	3 dB Bandwidth	900-1500 MHz minimum
	Gain ripple	<±0.5 dB, 950-1450 MHz
	Output impedance	75Ω
	Output return loss	>15 dB
	DC Power input	<180 ma at 12 volts
Power Supply Board	Maximum output current at:	
	+12 V -12 V +6 V	180 ma 180 ma 80 ma

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	Gain	>19.5 dB, 11.7-12.2 GHz
	3 dB Bandwidth	11.5 to 12.4 GHz minimum
	Gain ripple	<±0.25 dB, 11.7-12.2 GHz
	Input return loss	>10 dB
	Output return loss	>10 dB
	DC Power input	<80 ma at 6 volts
Mixer	Conversion loss	<6.5 dB, 11.7-12.2 GHz RF input
	RF return loss	>10 dB
	LO return loss	>10 dB
	IF return loss	>10 dB
Gunn Local Oscillator	Operating frequency	10.75 GHz ±4.0 MHz
	Output power	>20 mW
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	Gain ripple	<±0.5 dB, 950-1450 MHz
	Output impedance	75Ω
	Output return loss	>15 dB
	DC Power input	<180 ma at 12 volts
Power Supply Board	Maximum output current at:	
	+12 V	180 ma
	-12 V	180 ma
	+6 V	80 ma

3.0 INDOOR DEMODULATOR UNIT DESCRIPTION AND PERFORMANCE

3.1 GENERAL

The Indoor Demodulator Unit receives the downconverted RF signal from the Outdoor Downconverter Unit and demodulates the received signal at the selected channel to provide video and audio signals at their appropriate rear panel connectors. The input RF signal at J1 is between 950 to 1450 MHz and at a power level between -25 dBm to -55 dBm.

The assembly drawing for the indoor unit is shown in Figure 3-1. All RF and power connectors are located on the rear panel and the front panel contains the power on switch, channel select switches, and signal strength meter. The right side panel also contains two access holes to the potentiometers used to adjust the video and audio levels.

The rear panel connectors provide interfacing for all RF and power signals. J1 is the "F" type RF receptacle for the coaxial cable carrying the downconverted signal from the outdoor to indoor unit. J2 is the "F" type connector for the demodulated video output. The video output is designed for 75Ω transmission. TB1 is the terminal strip for the audio output connections and AGC level connections. The audio output impedance is 600 Ω balanced. The AGC level output is a dc voltage level that is indicative of the RF power level received by the outdoor unit. J3 is the output connector for mating with the power cable and is the output port which supplies the unregulated ±20 volts to the outdoor unit as well as the signal strength level. J4 is the AC power line input. The AC input is nominally 115V, 60 Hz, single phase, with a maximum power consumption of 25W.

The indoor unit assembly consists of the following internal subassemblies: the UHF microstrip tuner subassembly, the IF amplifirier subassembly,

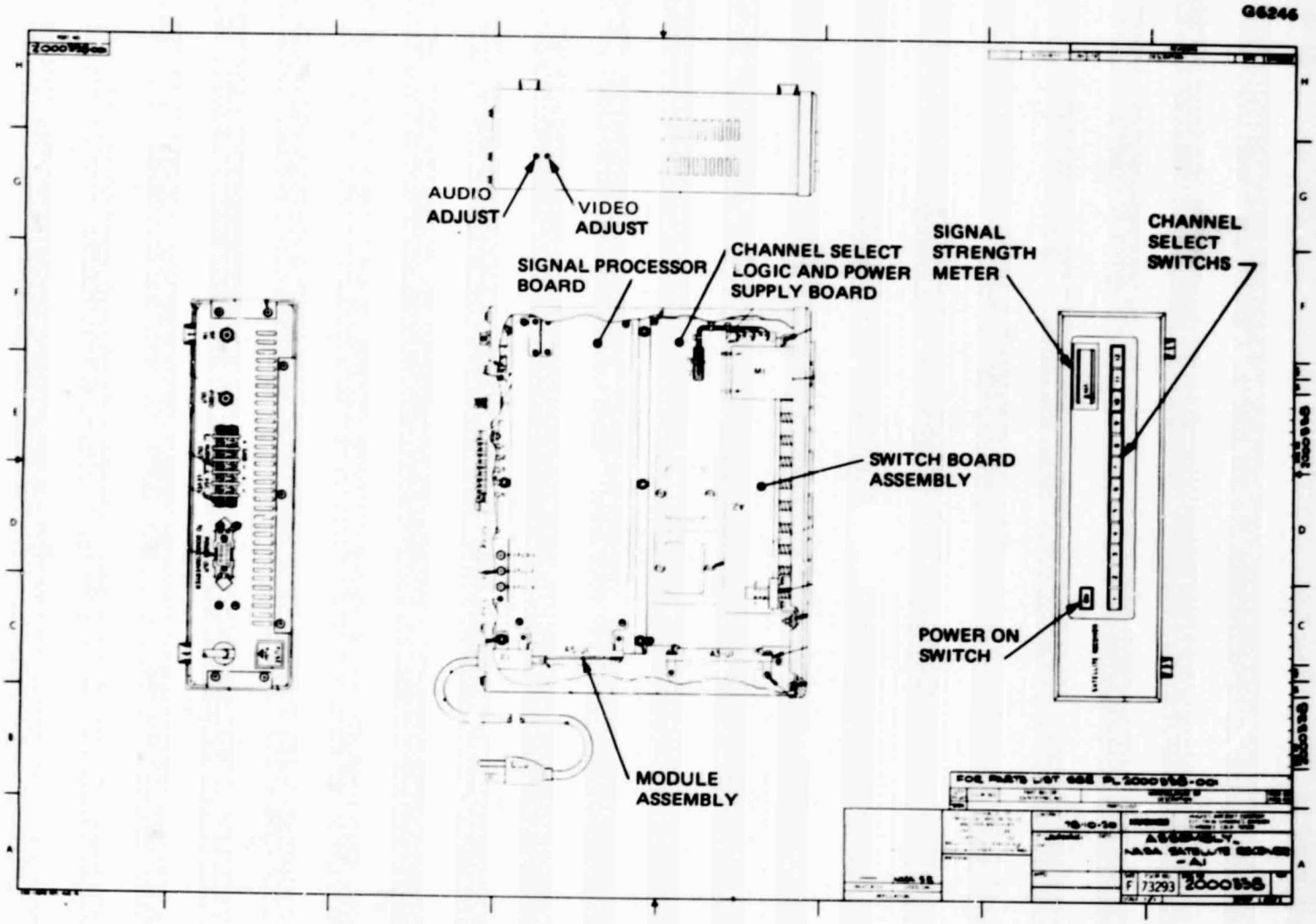


Figure 3-1A Indoor unit, assembly.

E2174

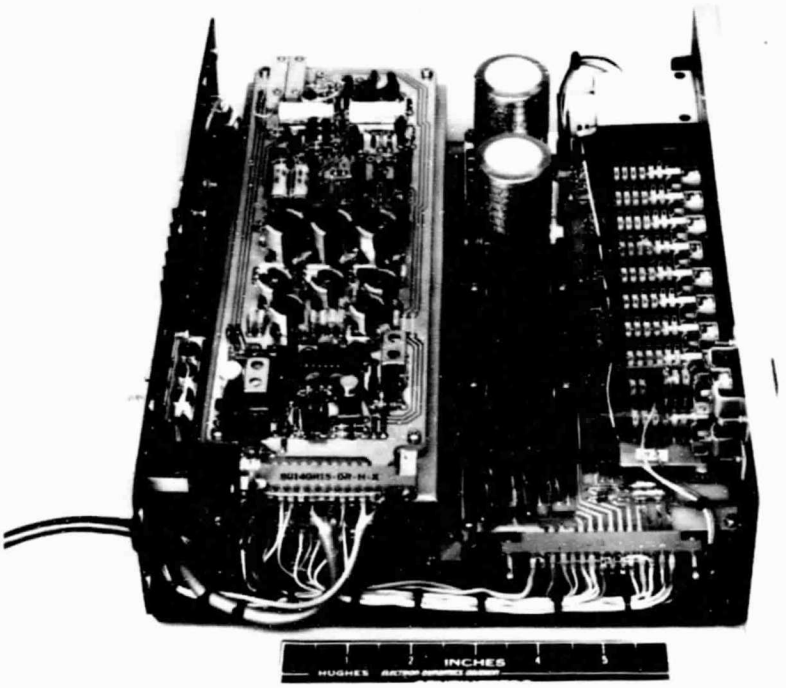


Figure 3-1B Indoor unit assembly.

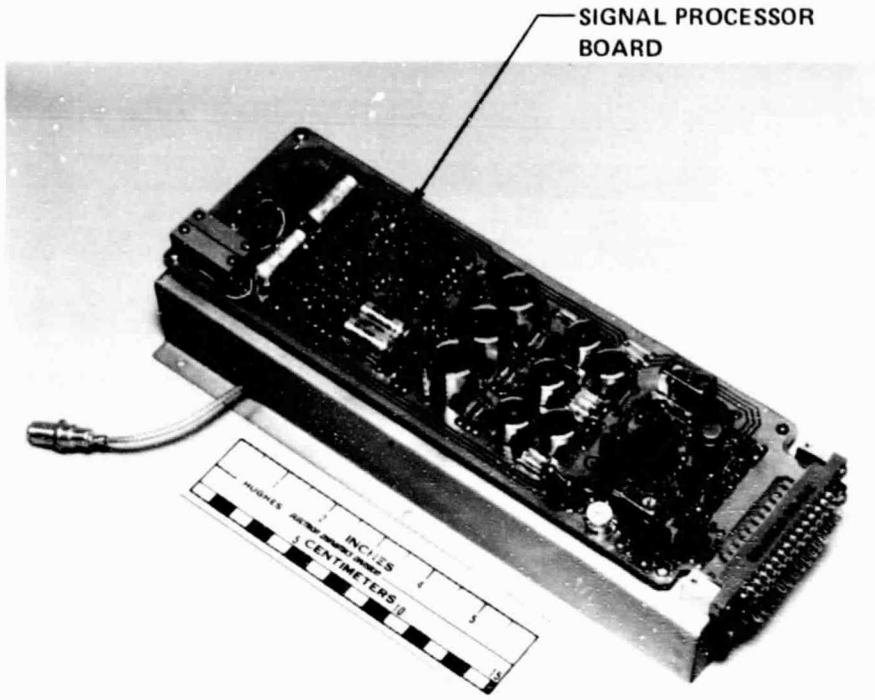


Figure 3-1C Indoor unit assembly.

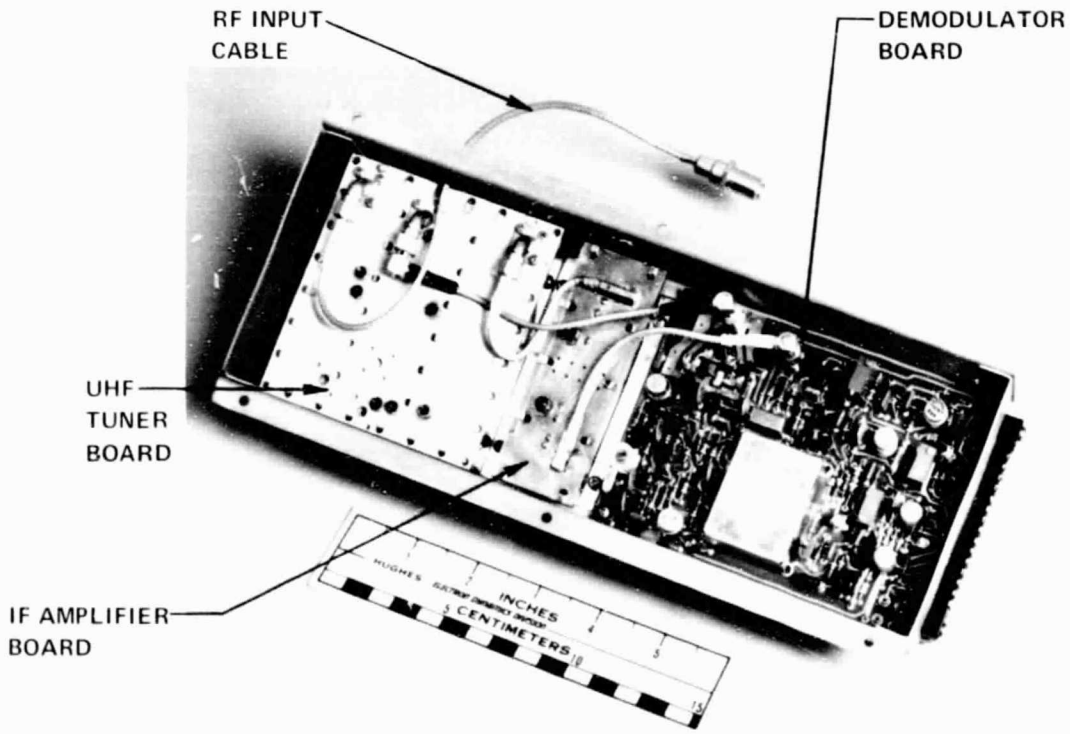


Figure 3-1D Indoor unit assembly.

the demodulator and sampler subassembly, the signal processor subassembly, the pushbutton assembly, and the channel select logic/power supply subassembly. The interconnection diagram between these subassemblies and the chassis mounted hardware in the indoor unit is shown in Figure 3-2. The description and performance of each of these subassemblies is presented individually.

Each board has a plug in connector and readily accessible test points to facilitate test and alignment of each board prior to final assembly of the indoor unit. Individual board testing will minimize troubleshooting time. Individual test fixtures will be used for each board.

3.2 UHF TUNER SUBASSEMBLY

3.2.1 Functional Description

The UHF tuner converts, filters and amplifies the signal obtained from the output of the outdoor downconverter unit. It gives frequency translation of 950-1450 MHz to the IF frequency of 300 MHz. The UHF tuner's assembly drawing and schematic are shown in Figures 3-3 and 3-4 respectively. The assembly consists of a printed microstrip board bonded to the backing plate with a conductive epoxy. The circuit components are assembled on the circuit side of the board and a metal can covers the top side of the circuits, thus yielding three shielded compartments for the least possible RF leakage.

Within the three compartments, the first section consists of a single stage RF amplifier followed by a voltage tuned bandpass filter and an attenuator. The second section contains a varactor tuned transistor oscillator which tunes from 1250 MHz to 1750 MHz, a double balanced mixer and a low pass filter which attenuates frequencies above the operating band of VCO. The third and last section consists of an IF amplifier and a five pole 300 MHz bandpass filter with a 30 MHz bandwidth.

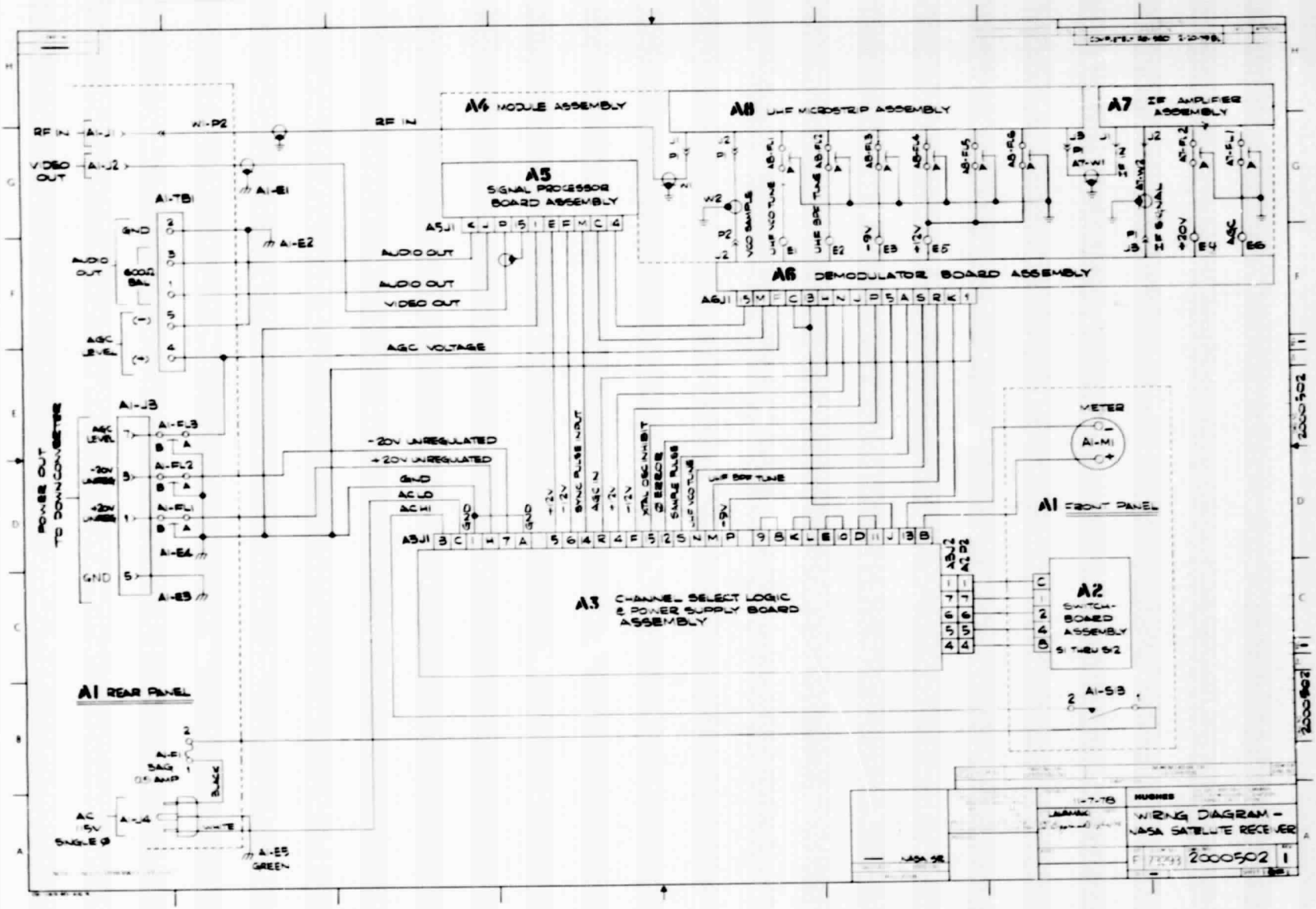


Figure 3-2 Indoor unit, wiring diagram.

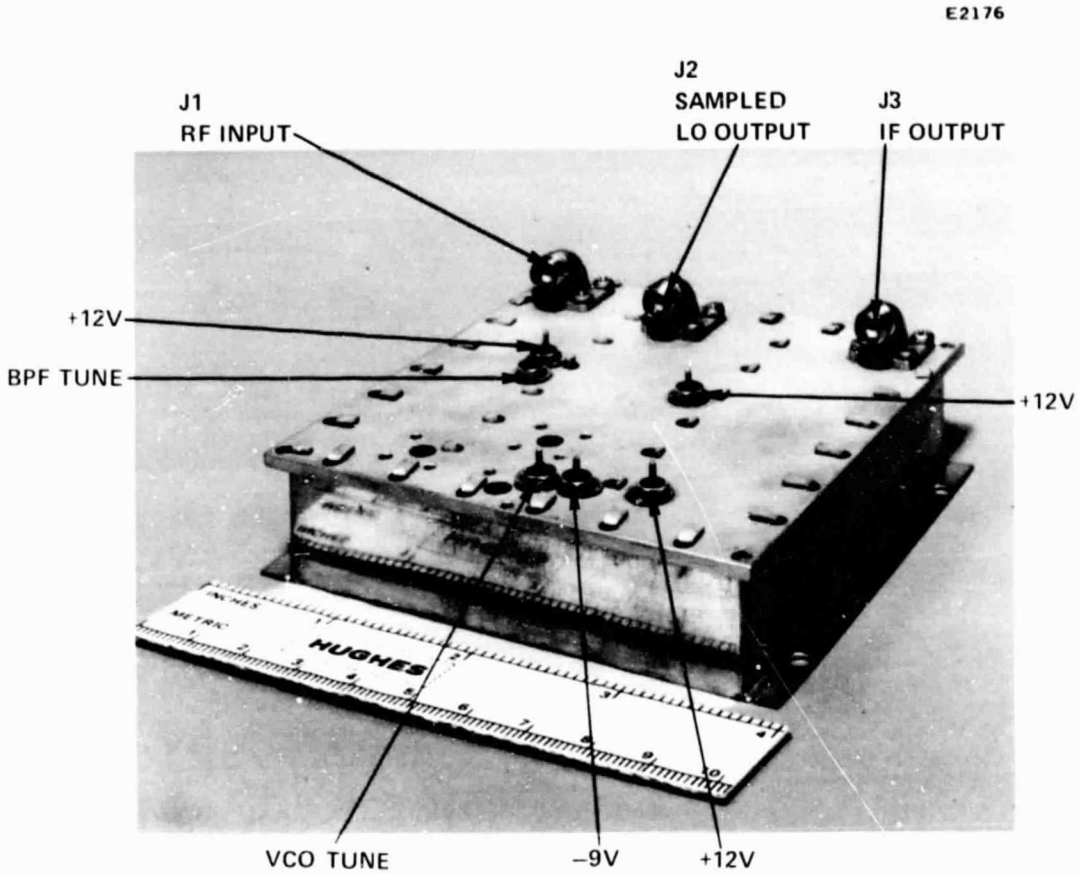


Figure 3-3A UHF tuner, assembly.

E2177

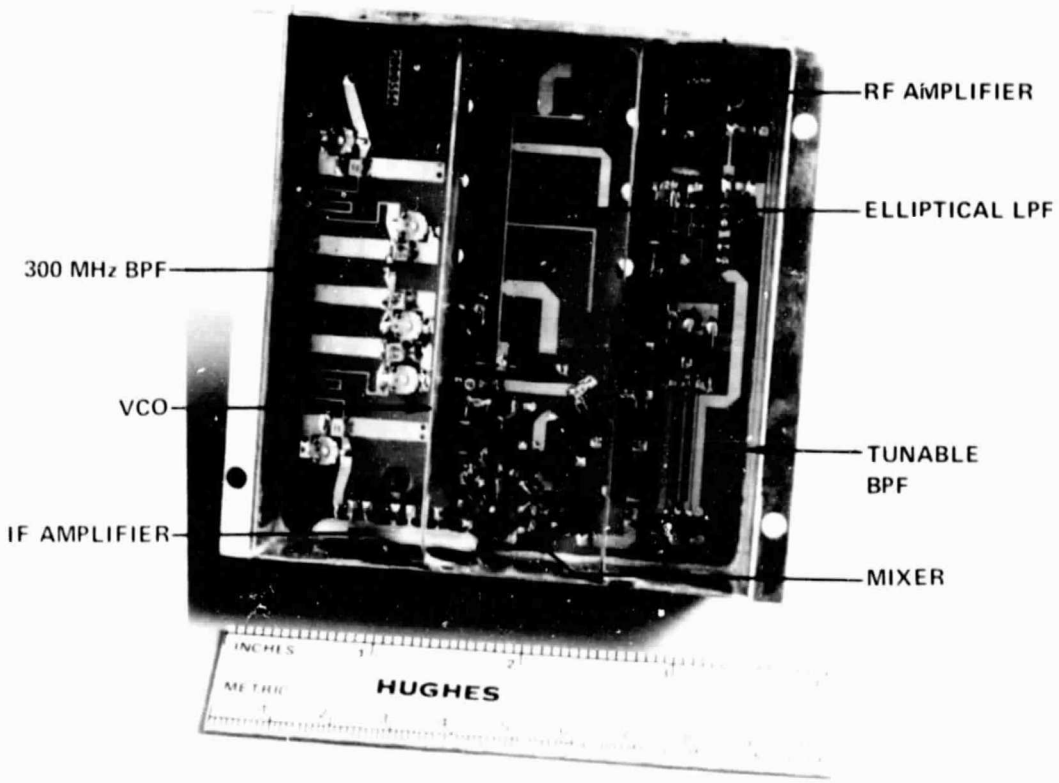


Figure 3-3B UHF tuner, assembly.

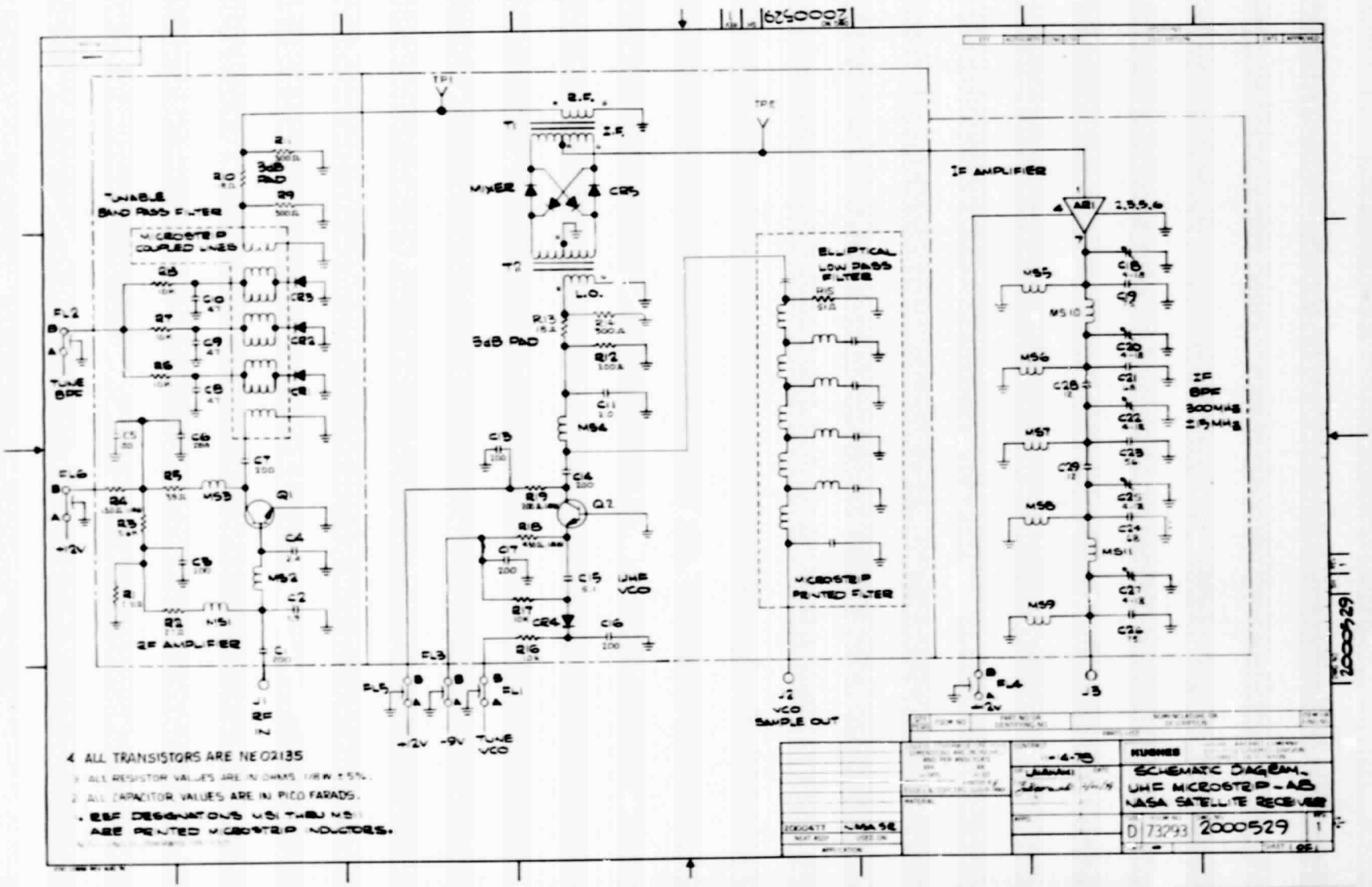


Figure 3-4 UHF tuner, schematic.

The RF input to the indoor unit, with a nominal level of -25 to -55 dBm, is directed to connector J1, the RF amplifier input on the UHF microstrip tuner. The RF signal achieves a nominal 10 dB gain and is applied to the voltage tuned filter. This filter has a nominal bandwidth of 200 MHz, a nominal insertion loss of 4.5 dB and is controlled by the channel select circuitry. This filter is tuned to the proper frequency by the channel select circuitry. The tunable BPF is required to reject those video channels which may interfere with the selected channel to generate an extraneous output at the 300 MHz IF frequency. The output of the filter is buffered by an attenuator preceding the RF port of the mixer. Figure 3-5 shows the RF input (J1) to RF section output (TP1) as a function of tuning voltage applied to the varactor tuned bandpass filter.

The LO/Mixer section of the UHF tuner converts the RF input to the mixer to an IF signal centered at 300 MHz. The local oscillator for the mixer is a varactor tuned transistor oscillator with the frequency of oscillation controlled by the channel select circuitry. A sample of the VCO output is coupled to an elliptical low pass filter, the output of which is directed to connector J2. This output sample is used by the tuner control system and a sharp attenuation skirt above 1740 MHz is necessary for proper tuner control. The tuning control system will be described with the Channel Select Logic subassembly. The typical VCO output at the mixer as a function to the VCO varactor tuning voltage is shown in Figure 3-6 along with the output of the elliptical filter at J2.

The downconverted IF signal at the IF port of the mixer is amplified with a nominal 13 dB gain and passes through the IF bandpass filter. This filter is a five pole microstrip filter at 300 MHz which establishes the receiver noise bandwidth at 30 MHz. The nominal microstrip IF response (TP2 to J3) is shown in Figure 3-7.

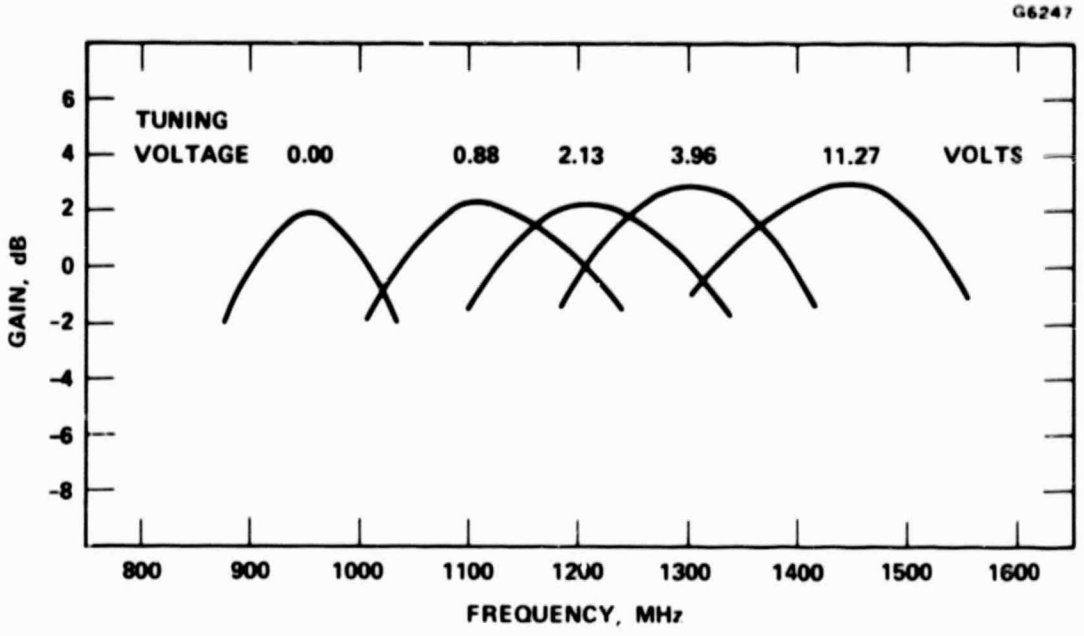


Figure 3-5 UHF tuner, tunable BPF response. J1 to TP1 as a function of tuning voltage.

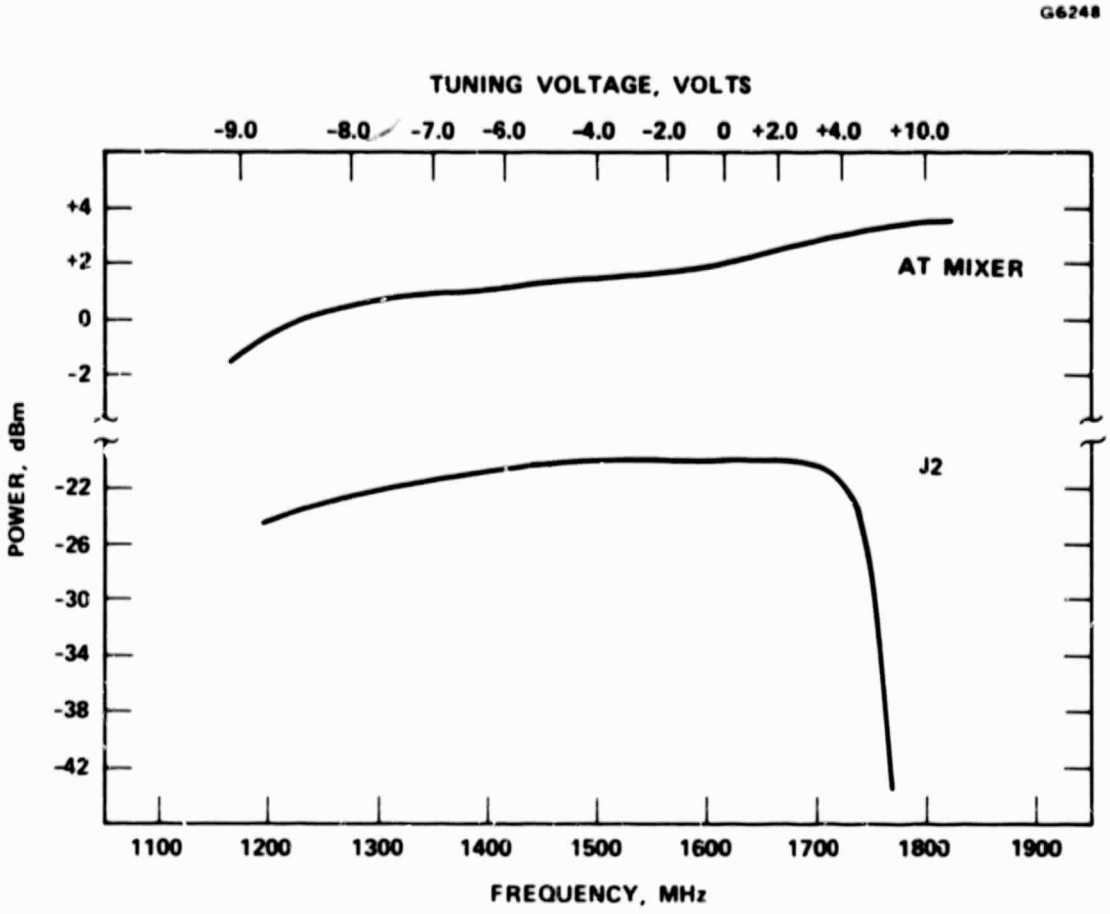


Figure 3-6 UHF tuner, VCO response. VCO output at the mixer and at J2 as a function of tuning voltage.

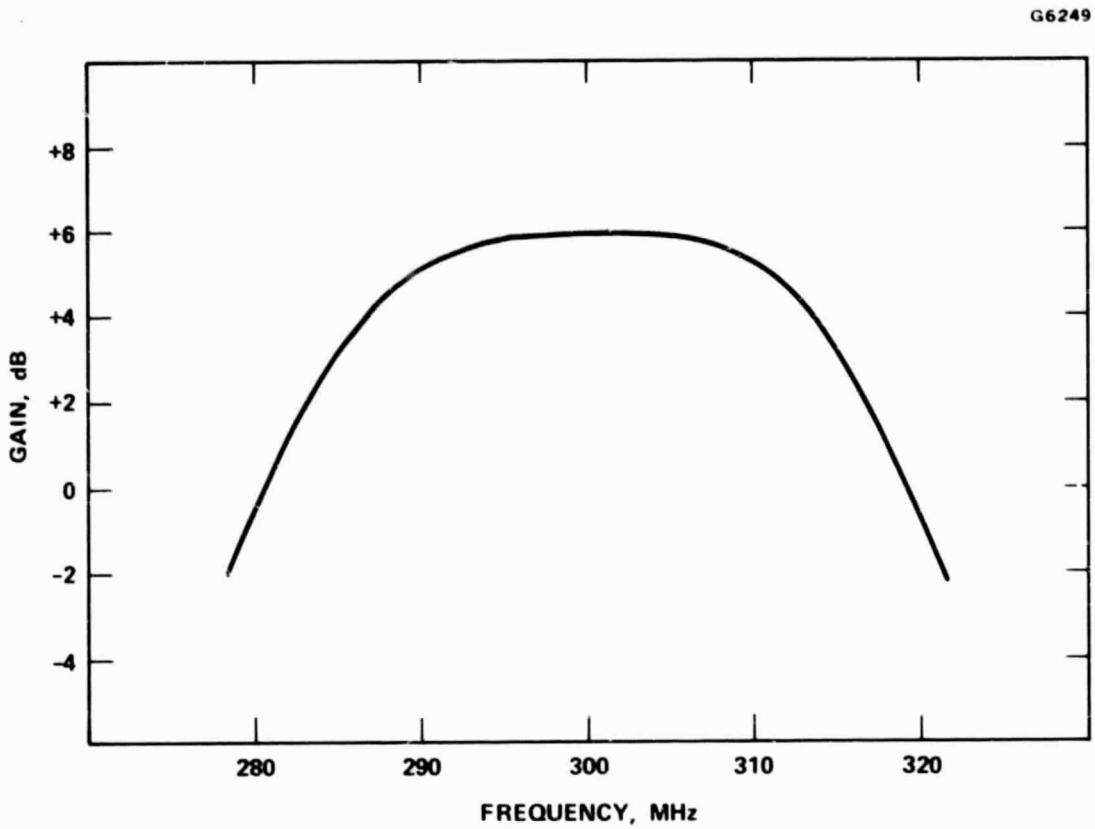


Figure 3-7 UHF tuner, IF response, TP2 to J3.

3.2.2 Alignment and Test

The UHF tuner must pass an alignment and test procedure prior to the final indoor unit assembly. To facilitate alignment and test, the tuner will be installed in a test fixture allowing efficient interfacing with the test equipment which will include frequency and voltage sources and waveform and voltage monitors. The only alignment necessary is the adjustment of the IF bandpass filter response. All other tests will involve monitoring the signal levels and VSWRs at all ports to verify proper operation. Signal injection and monitoring will be by connectors J1, J2, and J3 or by snap down RF probes at TP1 or TP2.

The IF bandpass filter is aligned by injecting a signal at TP2 and adjusting the five variable capacitors in the bandpass filter. The injected signal will be a swept frequency signal from 200 to 400 MHz at a power level of -30 dBm. The IF filter output at J3 will be monitored on a spectrum analyzer. By adjustment of the variable capacitors the test technician will center the IF response at 300 MHz and will obtain a nominal 3 dB bandwidth of 30 MHz. With the IF amplifier preceding the IF filter providing a nominal +12 dB gain, and with the nominal insertion loss of the IF filter at 6 dB, the test technician will measure a nominal +6 dB gain from TP2 to J3.

There are no other adjustments necessary with the rest of the tuner, but the tuner must pass a series of Go/No Go functional tests. The RF section is tested by applying to port J1 a frequency signal varying from 900 to 1500 MHz at a power level of -35 dBm and the RF section output at TP1 is monitored on a spectrum analyzer. The test technician will verify that the bandpass filter tunes from 950 MHz to 1450 MHz, with a nominal bandwidth of 200 MHz, as the tuning voltage is varied from 0 to +11 volts. The amplifier preceding the filter provides a nominal +10 dB gain and the insertion loss of the filter is nominally

4.5 dB. With the additional 3 dB loss in the output resistive pad, the nominal gain from RF input at J1 to RF output at TP1 is +2.5 dB.

The LO/Mixer section of the UHF tuner must also pass a series of tests. The VCO is swept from 1200 MHz to 1800 MHz by sweeping the tuning voltage from -9 volts to +10 volts. The elliptical lowpass filter output at J2 is monitored on a spectrum analyzer. The test technician will verify that the power level is -22 dBm ±2 dB for frequencies below 1720 MHz and is less than -35 dBm for frequencies greater than 1760 MHz. The filter response is much more dependent on the dielectric constant of the teflon fiberglass board than on etching tolerances. To obtain the proper response, the dielectric constant is specified to be 2.45 ±0.04. As the VCO is swept, the mixer performance is evaluated by monitoring the mixer IF output at TP2. An RF source is connected to J1 and its frequency sweep is made to track the VCO output at J2 so that there will appear a constant frequency of 300 MHz at the mixer output at TP2. By noting the RF and IF power levels the converion loss of the mixer, as observed over the swept frequency inputs, must be verified to be less than 8 dB.

As the final test the RF input and IF output of the UHF tuner are verified to have VSWRs less than 1.43 (return loss greater than 15 dB).

3.3 INDOOR IF AMPLIFIER SUBASSEMBLY

3.3.1 Functional Description

The IF Amplifier subassembly receives the IF signal from the microstrip tuner and amplifies it to the proper level for use in the Demodulator board. The IF amplifier subassembly consists of two shielded stages of amplification, the first stage of which is used for the AGC function. The schematic of the IF amplifier is shown in Figure 3-8 and the assembly is shown in Figure 3-9. By varying the bias voltage to the first IF amplifier stage, gain control is achieved.

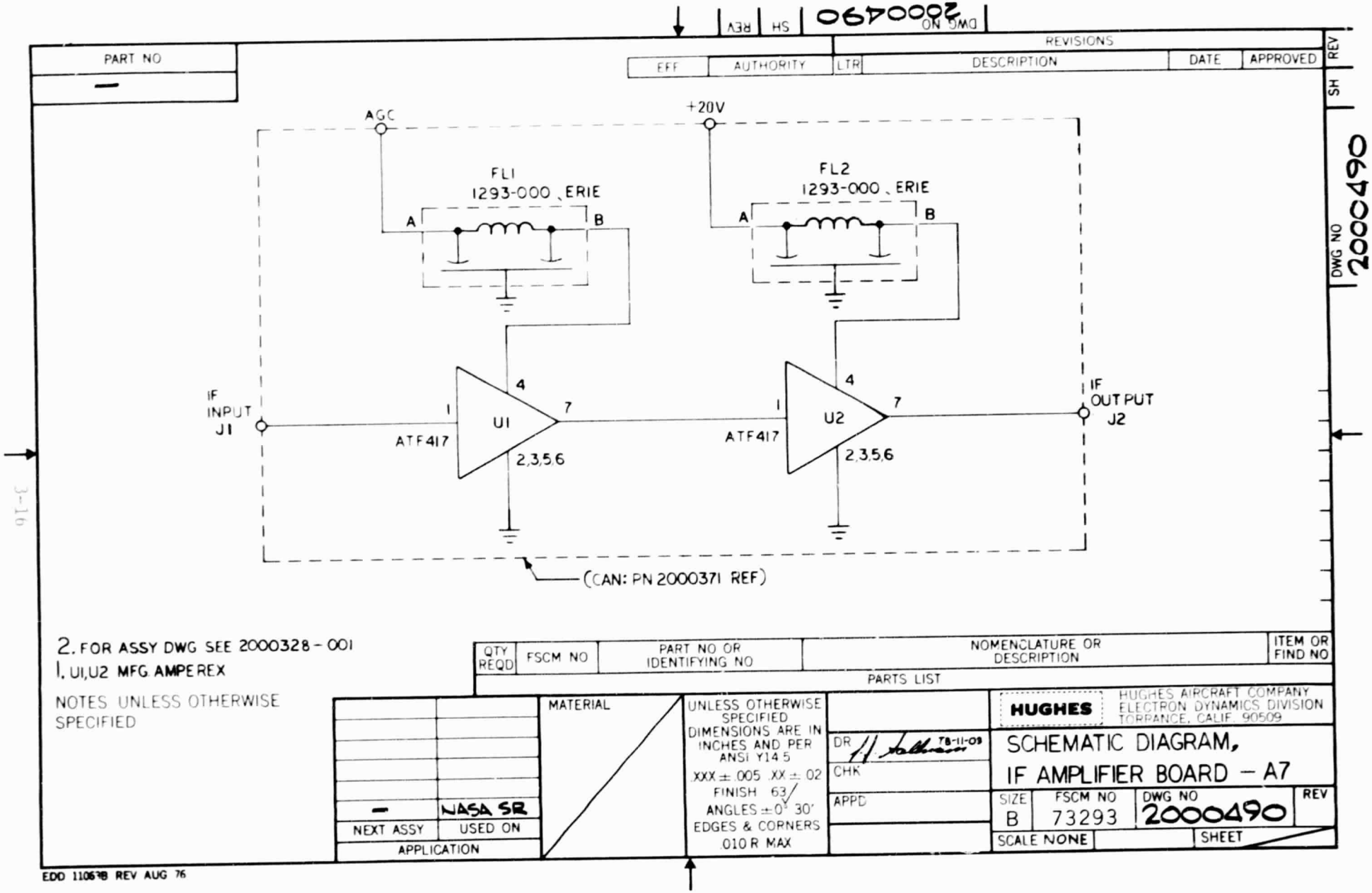


Figure 3-8 Indoor IF amplifier, schematic.

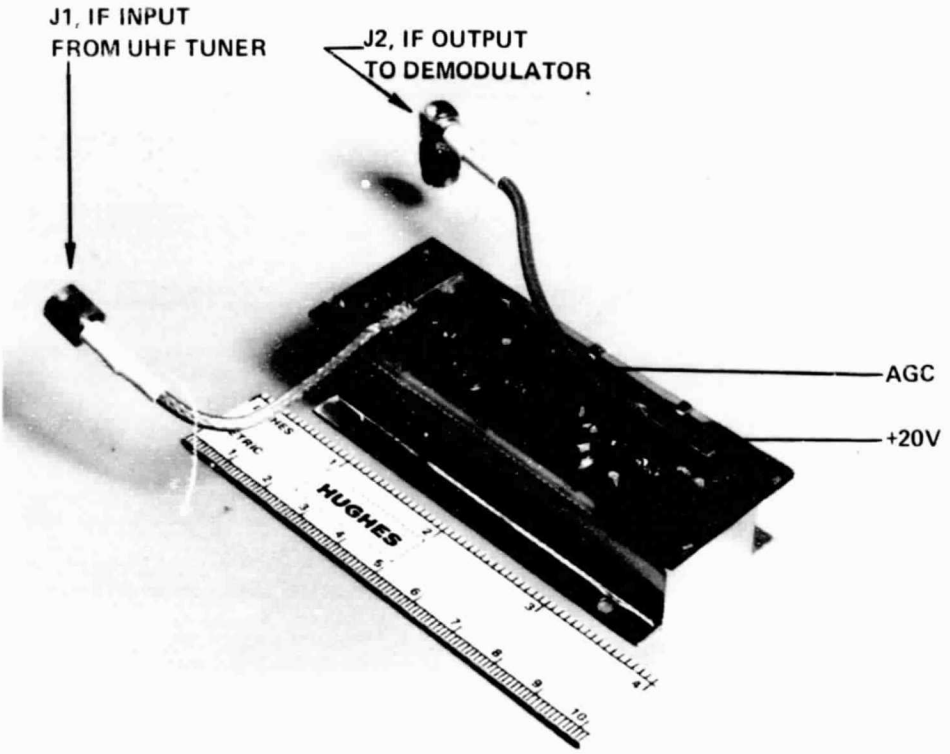


Figure 3-9A Indoor IF amplifier, assembly.

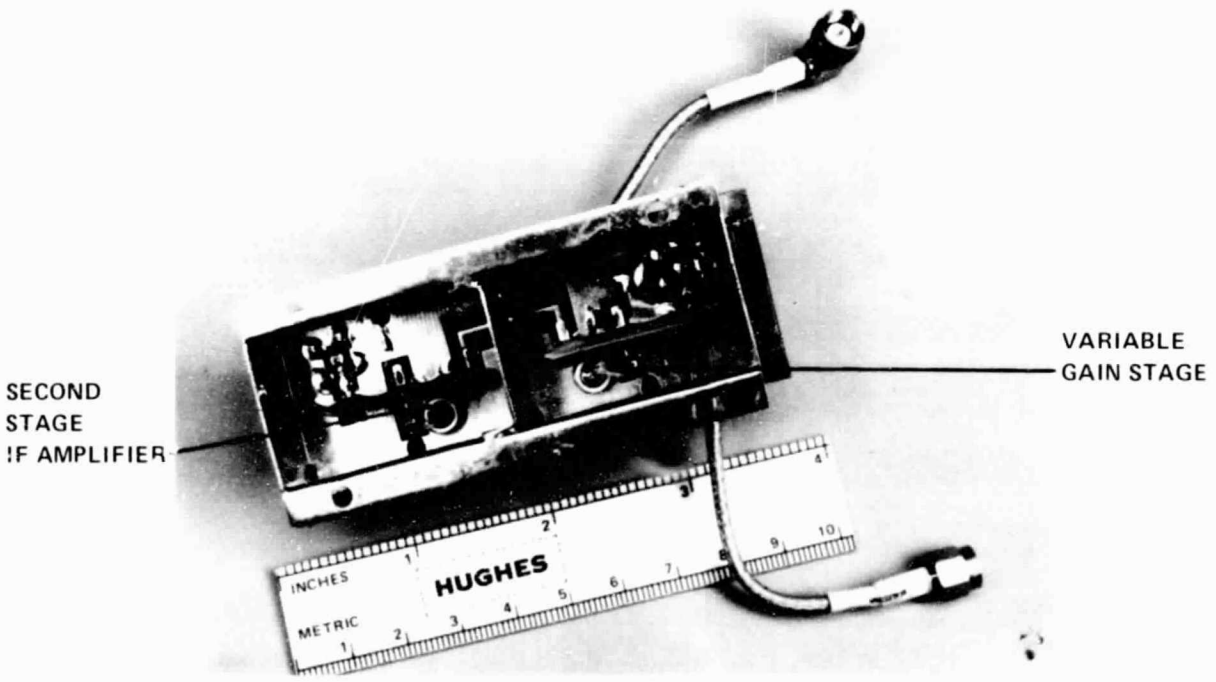


Figure 3-9B Indoor IF amplifier, assembly.

Figure 3-10 shows the gain of the IF amplifier subassembly as a function of AGC voltage. As can be seen, AGC action is achieved over a 30 dB range.

3.3.2 Test

The indoor IF amplifier subassembly has no alignment required and is tested to verify proper AGC operation. With an input signal at 300 MHz, the test technician will verify that the power gain is greater than 50 dB and that the 1 dB gain compression point occurs at an output power level greater than 0 dBm. The AGC voltage will be varied to verify that greater than 25 dB of gain control can be obtained. These tests will consume a minimal of time.

3.4 SIGNAL PROCESSOR SUBASSEMBLY

3.4.1 Functional Description

The signal processor board separates the demodulated video information from the unprocessed audio signal, processes the video and audio signals, and provides a 1.0 volt p-p adjustable video output signal and a 0 dBm adjustable audio output signal. The schematic for the signal processor board is shown in Figure 3-11 and the assembly is shown in Figure 3-12.

The composite video signal input is applied to a 6 dB 75Ω resistive power splitter, R1, R2, R5. This splitter performs two functions. It applies the video and audio signals to their respective filter networks and insures proper impedance loading to these filters.

The video signal is first passed through a 5.14 MHz band reject filter which is used to attenuate the audio subcarrier while passing the demodulated video information. This network provides a nominal 30 dB of attenuation at 5.14 MHz but has negligible attenuation at the video frequency.

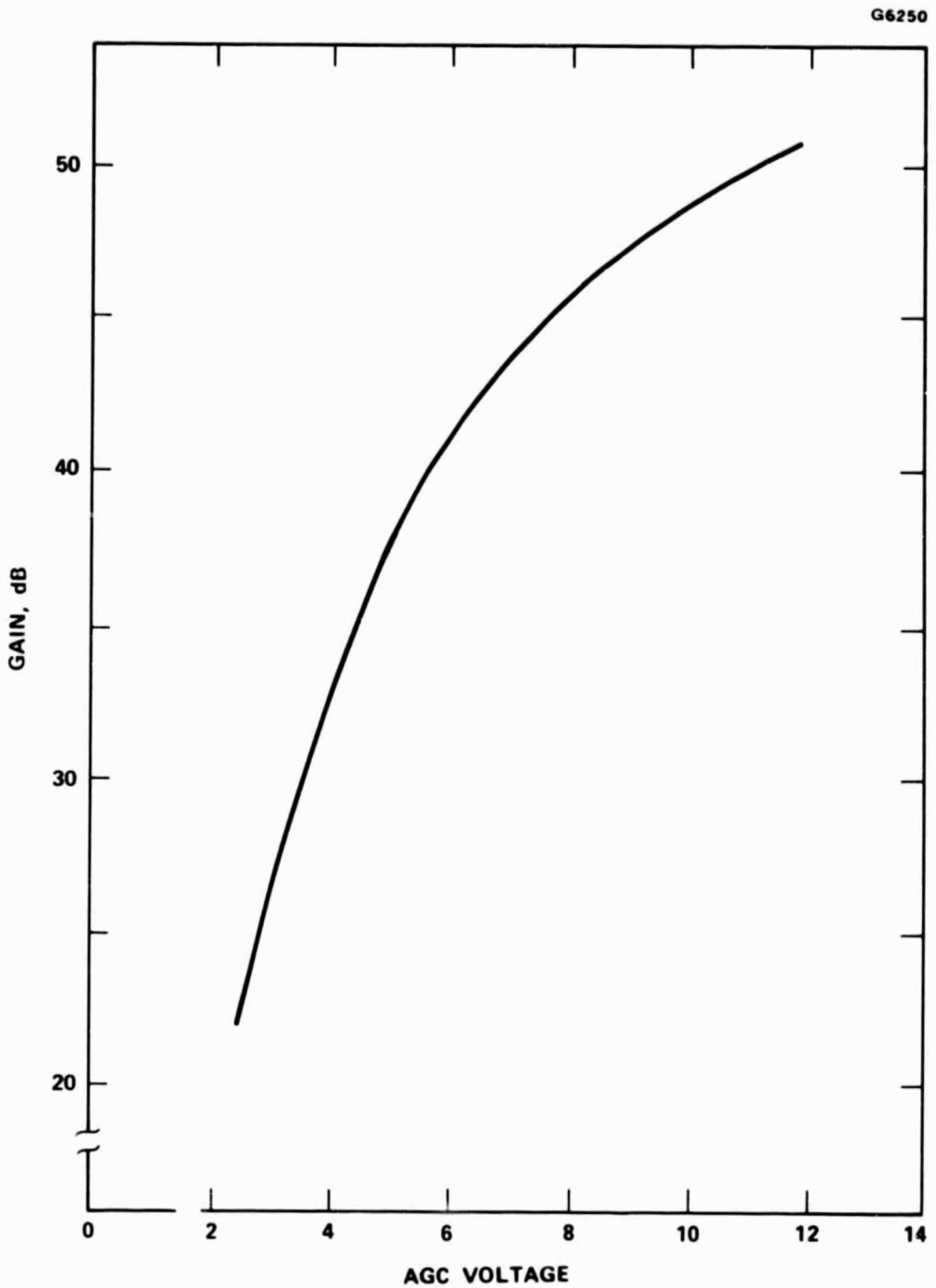


Figure 3-10 Indoor IF amplifier, AGC response.

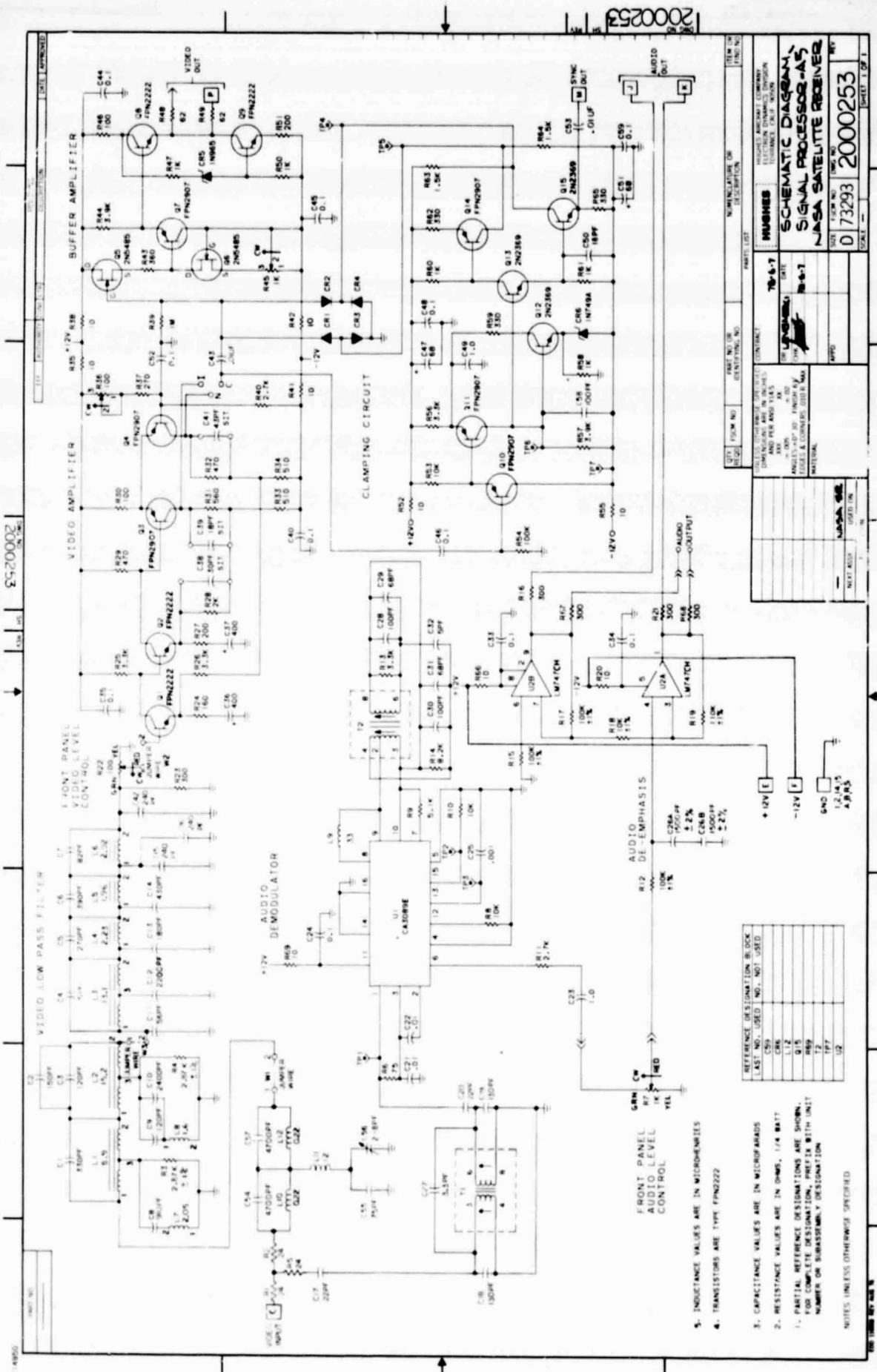


Figure 3-11 Signal processor board, schematic.

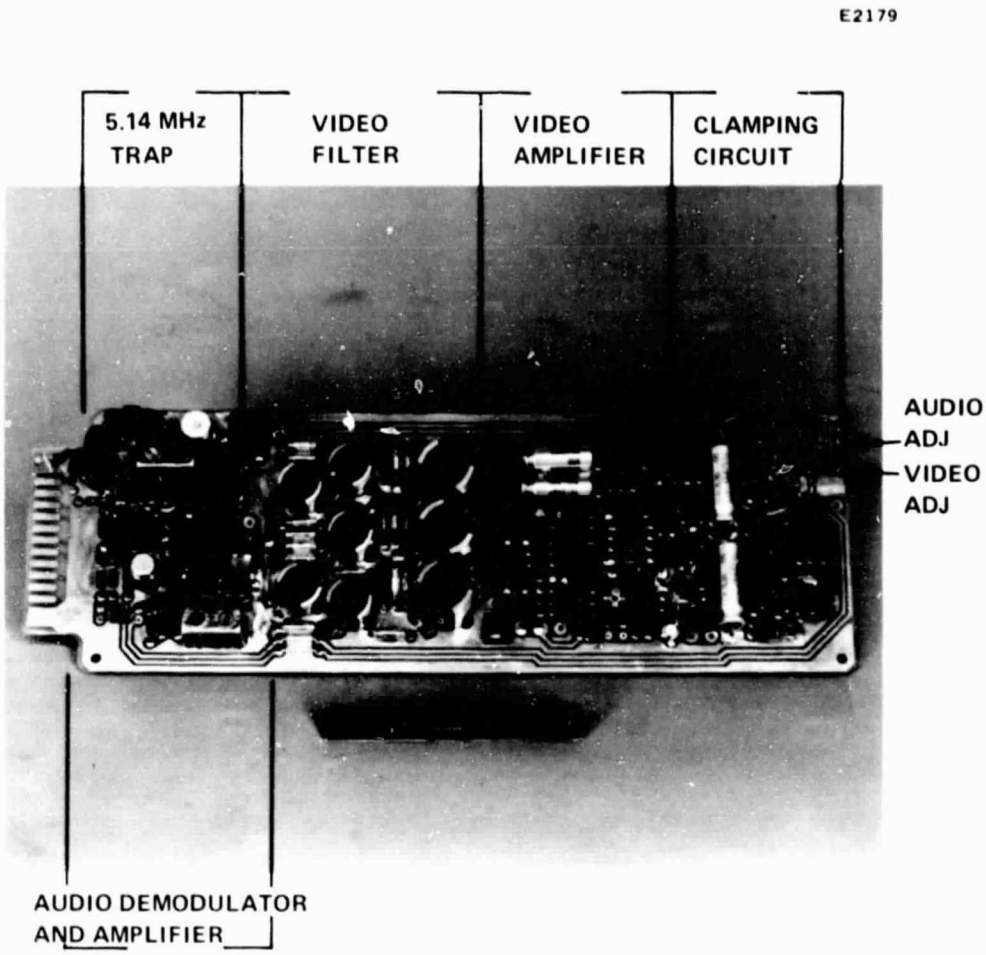


Figure 3-12 Signal processor board, assembly.

This network is necessary due to the audio sub-carrier frequency being only 940 KHz above the video base band frequency. Without it, the video signal to noise ratio would be degraded and visual picture distortion would occur. The output of the 5.14 MHz reject filter is connected to the input of the video low pass filter. This filter has a phase equalization network which serves to linearize the phase response of the low pass filter. The low pass filter accomplishes several important functions. First, it sets the received video bandwidth for computing the theoretical signal-to-noise ratio of the received video signal. Second, the low pass filter provides an additional 12 dB attenuation to the audio subcarrier signal that is in the composite video signal.

The output of the low pass filter is connected to a four transistor video amplifier through a potentiometer, R22, which controls the video level. This amplifier has approximately 30 dB gain over the complete video spectral range. Included in the amplifier are three select-in-test capacitors that are used to optimize the frequency response and stabilize the amplifier from ringing. This amplifier drives a buffer amplifier consisting of three bipolar transistors and two junction FETs. The buffer amplifier has a 75Ω output impedance and unity gain and a stable dc bias over temperature.

Also included in the video circuitry is a sync separator circuit, a sync pulse amplifier and a video clamping circuit. The sync separator, Q11 and Q12, removes the video sync pulses from the video signal. The sync pulses are then amplified by Q13, Q14 and Q15 and fed to the clamping diodes, CR1 through CR4, which clamps the video signal to ground during sync time. This clamping action forces a charge on the video coupling capacitor connected to the input of the video output buffer stage such that dc restoration is obtained at the video signal. In addition this clamping action removes the 30 Hz energy dispersal signal normally present in the satellite system.

The 30 Hz energy dispersal signal is a triangular waveform applied to the modulated 12 GHz signal at the earth transmit terminal prior to relay by the satellite. The energy dispersal function typically modulates the RF carrier at less than 10% of the maximum deviation of the carrier by the video signal. This action spreads the power content of the RF carrier over a broader frequency spectrum so as to minimize any adverse interference with other terrestrial communications links. At the receiver, the energy dispersal action results in a demodulated video signal with a sync pulse voltage reference level that follows a triangular waveshape at the frame rate period. The clamping circuit detects the presence of the sync pulses in the video waveform and restores the sync pulse reference level to zero volts. These waveforms are shown in Figure 3-13. The clampling action not only rejects the 30 Hz triangular waveshape due to the RF transmitter energy dispersal, but also removes 60 Hz and harmonic ripple that may be added to the video signal due to ripple on the power supply lines. The clamping action will occur regardless of whether or not energy dispersal is present on the transmitted RF signal.

The audio signal processing begins by separating the video signal from the audio subcarrier through the 5.14 MHz band pass filter, T1, at the input to the signal processor board. The audio subcarrier is applied to an integrated circuit, U1, used for FM demodulation. The integrated circuit includes an IF amplifier, limiter, quadrature detector, and audio preamplifier. This circuit has a wide dynamic range and low audio distortion. The output of the demodulator is passed through an audio level control, R7, a 75 μs de-emphasis network consisting of R12 & C26, and into a wideband low distortion bridge amplifier, U2. This amplifier uses a pair of operational amplifiers with a large feedback ratio to minimize audio distortion while simultaneously obtaining wide audio response. The output impedance of this bridge amplifier is 600Ω, and is capable of driving loads lower than 600Ω if necessary.

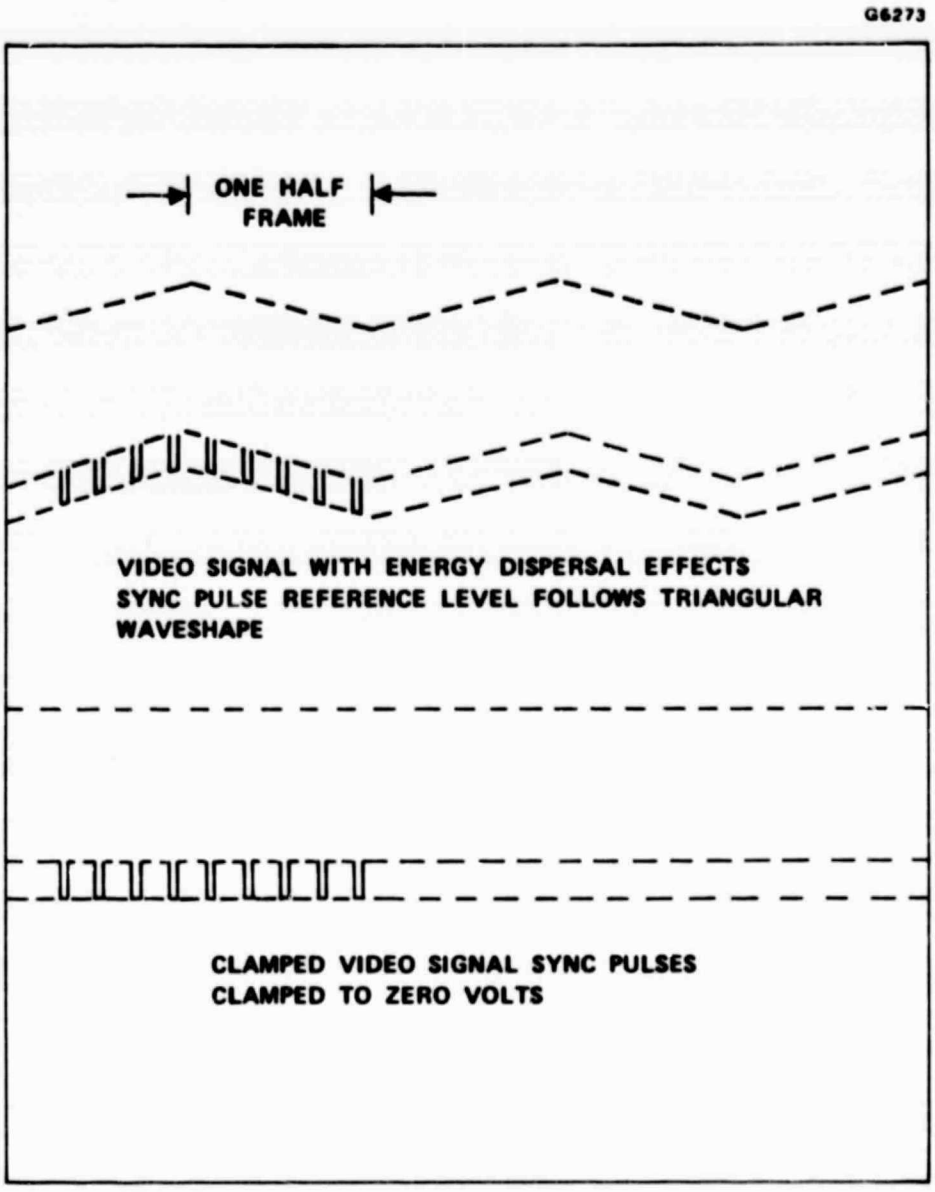


Figure 3-13 Resultant video signal, clamped or unclamped, with energy dipersal applied to the RF transmitter.

3.4.2 Alignment and Test

The signal processor board requires proper alignment for satisfactory video and audio performance. The board has convenient test points and plug in wire jumpers to facilitate test signal injection and monitoring. A test fixture will be designed to simplify all interfacing with the board during test and alignment and to minimize the required test time. The video and audio alignment procedure is as follows:

VIDEO ALIGNMENT

With $\pm$12 volts applied to the board, input a 1 V_{p-p} 5.14 MHz signal to the composite video input, and unplug the jumper, W1, between the band reject filter and the video low pass filter. This filter must be loaded with 75Ω as seen looking into video low pass for adjustment. Adjust C56 to minimize the signal amplitude (less than 30 mV_{p-p}). Plug back in the jumper wire. Disconnect the 5.14 MHz signal.

Using an NTSC 147 video generator, input a 1 V_{p-p} video combination test signal at the video input. Unplug the jumper, W2, at the output of the video low pass filter and monitor the video filter output on an NTSC vector scope and a waveform monitor with R22 turned fully clockwise. Set the adjustments on L1 thru L8 to midrange. Adjust L4, L5, and L6 for the flatest response on the waveform monitor to a multiburst signal. Some interaction may occur in the turning of the inductors, necessitating alternating between the adjustments until an optimum response is obtained.

Now switch the video signal to the composite test signal with the 12.5T pulse and measure the chrominance to luminance delay inequality. Inductors L7, L8, L1, L2, and L3 are now adjusted to minimize the chrominance to luminance delay. Some interaction between inductors may occur necessitating several iterations until optimum results are obtained. At

this point the video generator should be switched back to multiburst and the frequency response rechecked. If readjustment is necessary the phase linearity should also be rechecked.

Re-install the jumper, W2, between the video level control and the input to the video amplifier and disconnect the composite signal input. Install the jumper between the non-inverting output of the video amplifier and the buffer amplifier input. R36 is adjusted until a reading of 0 VDC is obtained on the collector of Q4. R45 is adjusted for zero volts DC at the video output. With the composite signal input to the board the video output signal is observed on the video monitor. The capacitor C41 is selected for optimum frequency response and plugged into its appropriate sockets.

This completes the adjustment of the non-inverting portion of the video amplifier. To optimize the inverting output of the video amplifier the input video signal is inverted. Remove the jumper wire between the non-inverting output and the buffer amplifier input and install a jumper between the inverting output and the buffer input. Capacitor C39 can now be optimized for best frequency response in the inverting mode.

While observing the video output on the monitor, capacitor C38 can be selected to provide minimum ringing at the bar of the video signal.

At this point only the clamp circuit needs to be tested to verify proper operation. With energy dispersal applied to the input composite signal, place a jumper wire from TP6 to TP7 and observe that the video output becomes unclamped. Jumpering TP6 and TP7 effectively disengages the clamping circuit by disabling Q12, Q13, Q14 and Q15. The video waveshape then observed on the video monitor will follow a 30 Hz triangular waveshape. With TP6 and TP7 disconnected, the clamping circuit will be engaged and the video signal signal will be observed to acquire dc

restoration. This completes the test and alignment of the video section of the signal processor board.

AUDIO ALIGNMENT

With the ±12 volts power on at the signal processor board, apply a 5.14 MHz signal to the composite video input. This signal should be 150 mV p-p and be FM modulated with a 1 KHz tone with ±60 KHz deviation. With a high frequency scope probe connected to TP1, adjust both T1 adjustments for maximum amplitude and signal centered in its filter response. Now, decrease the input signal to 15 mV p-p and connect an RMS voltmeter (600 Ω) to the audio output. Adjust T2 for maximum audio output, decreasing R7 to ensure that the audio output is not clipping due to overdrive.

The audio signal must undergo pre-emphasis before modulating the audio carrier. The audio output level from the signal processor board should be flat within ±2 dB over the frequency region.

This completes the video and audio alignment of the signal processor board. This simplified alignment procedure will result in a video and audio performance within the present specifications. However, with a more involved test and alignment procedure this circuit is capable of meeting the more stringent CATV standards per EIA standard RS-250.

3.5 DEMODULATOR SUBASSEMBLY

3.5.1 Functional Description

The demodulator board actually contains three separate functions, the phase lock loop demodulator, the AGC circuit, and the sampler circuit. The functional description of these circuits is presented here. The schematic and assembly drawing are shown in Figures 3-14 and 3-15.

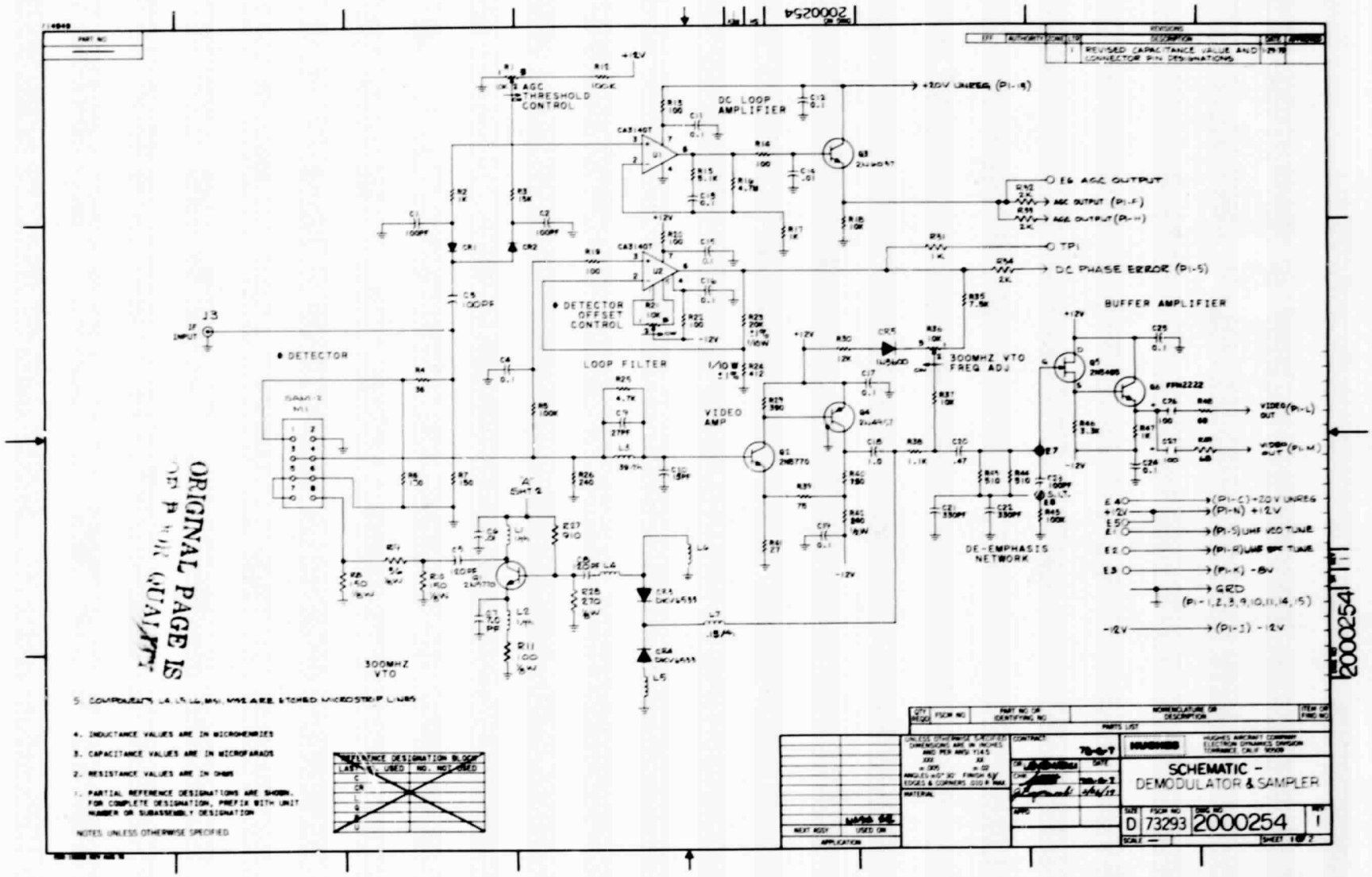


Figure 3-14A Demodulator board, schematic.

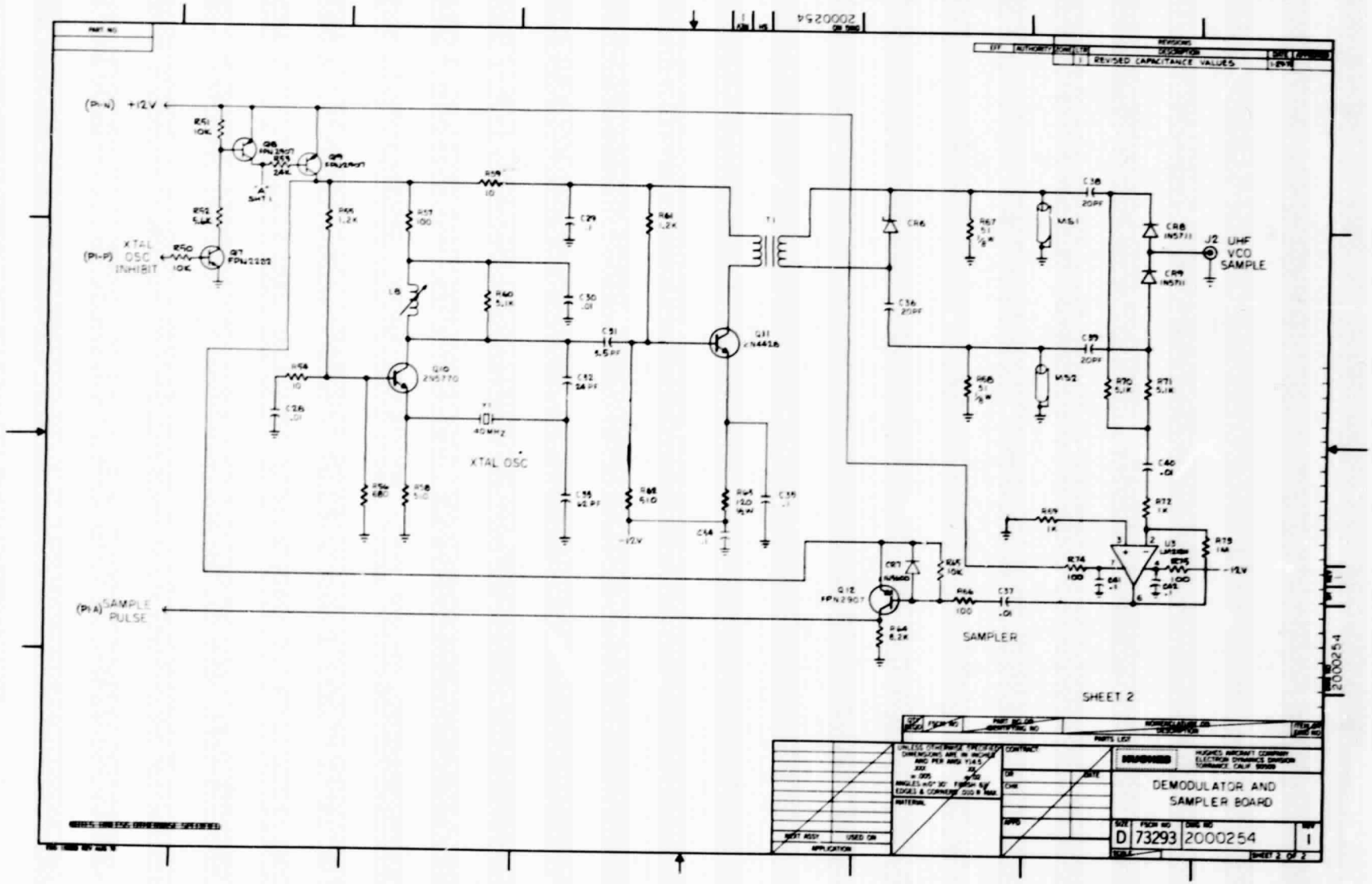


Figure 3-14B Demodulator board, schematic.

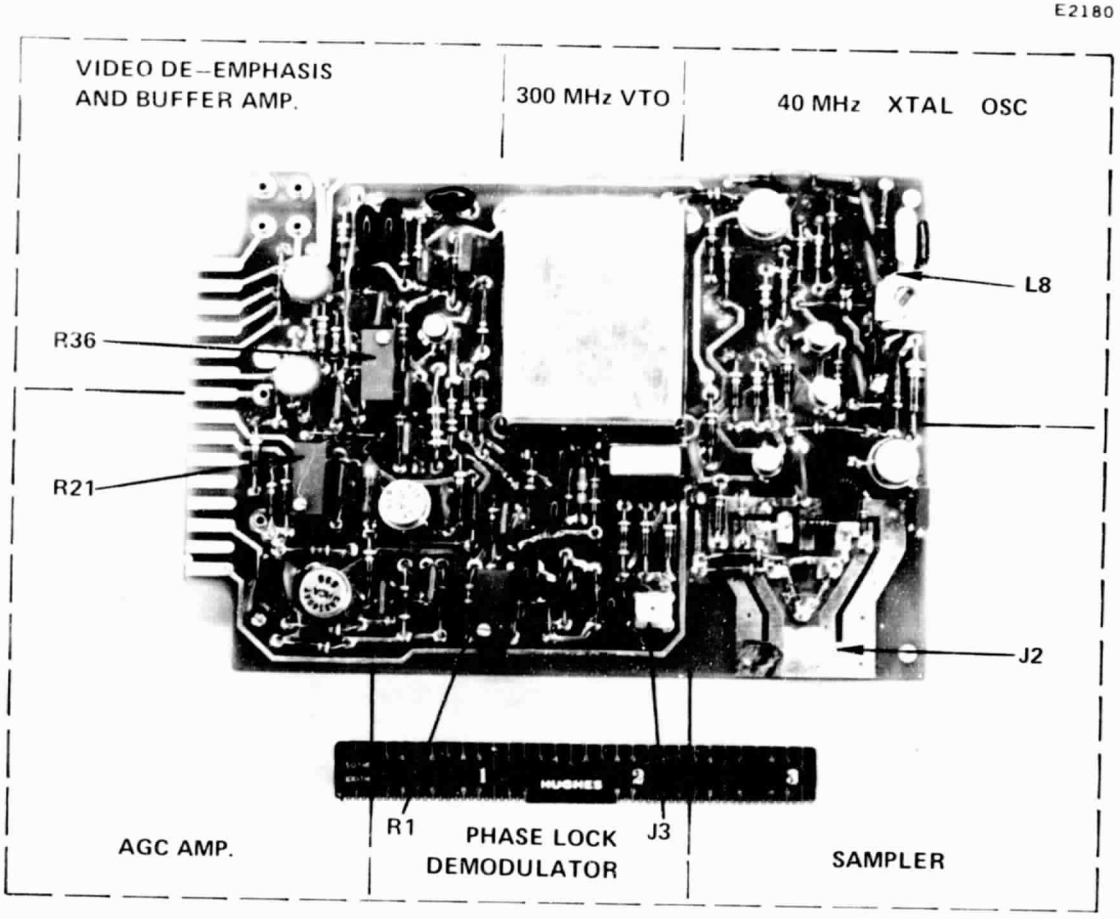


Figure 3-15 Demodulator board, assembly.

The IF input to the demodulator board at J3 is directed both to the AGC detector diodes and through a 6 dB pad to the phase detector. This input level is nominally -6 dBm which is within the sensitivity range of the AGC detectors and will enable proper AGC tracking in response to IF power variations. It also is the correct level for the phase detector to obtain the optimum phase lock loop gain.

The AGC circuit consists of the AGC detector and the AGC amplifier. The detector, CR1 and CR2, consists of two low level zero bias Schottky diodes which rectifies a sample of the input IF signal at J1. The rectified level is compared to the adjusted threshold level at R1 and drives the high gain op-amp U1 and power amplifier Q3. The AGC output signal at A6 is applied to the IF amplifier U1 on the IF Amplifier Board causing the IF gain to increase or decrease as required to drive the rectified IF level towards the level of the threshold adjustment.

The IF input to the demodulator board is also directed through a 6 dB pad to the phase lock loop (PLL) which demodulates the composite signal from the incoming IF signal at 300 MHz. The input level is attenuated by 6 dB to bring the power level within the range for proper phase lock loop operation. The phase detector output is a phase error voltage which is a function of the phase difference between the input IF signal and the onboard 300 MHz VTO local oscillator.

The phase error output of the phase detector drives two loop amplifiers. The low frequency loop amplifier is an operational amplifier, U2, with a cut-off frequency at 100 Hz. The wide bandwidth video loop amplifier Q4 and Q2 has its frequency response controlled by its input loop filter. The output of the video loop amplifier is capacitively coupled to a summing network with the low frequency loop amplifier output.

This loop amplifier output voltage is the demodulated composite video signal. It is also the error voltage applied to the 300 MHz VTO to

drive the loop to the phase lock condition. This demodulated signal is passed through the de-emphasis filter and then through output buffer amplifier Q5 and Q6.

The sampler circuit on the demodulator board mixes the sample input at J2 with the harmonic of a 40 MHz oscillator and sends out a sample pulse whenever the UHF microstrip VCO sweeps past a 40 MHz harmonic. The oscillator, at Q10, has its output tuning element at L8. The 40 MHz oscillation is amplified by the power amplifier, Q11, whose output drives the step recovery diode, CR6, to generate the 40 MHz comb spectrum. The mixer output is amplified by the fast op amp U3. The sample pulses are amplified by the pulse amplifier Q12, providing the proper level to the channel select logic board.

The channel select logic controls the state of the "XTAL OSC INHIBIT" input. When low, this input acts to turn off the 300 MHz VTO and turn on the 40 MHz oscillator. This state exists during the receiver tuning mode of operation. When high, the XTAL oscillator is turned off and the 300 MHz VTO is turned on. This condition exists during the demodulation of the video and audio program.

3.5.2 Alignment and Test

The various controls of the demodulator board must be adjusted for optimum performance. These adjustments are made during the board initial test and alignment. The following is a description of the alignment procedure for the various controls.

The test fixture will contain the necessary interfaces as well as an IF amplifier with AGC provision so that the AGC circuitry can be tested in a closed loop operation. With $\pm$12 volts supplied to the Demodulator board, a 300 MHz signal generator at -40 dBm power level is connected to the IF amplifier which then feeds the demodulator input J1. The

AGC voltage output is applied to the AGC terminal of the IF amplifier. By adjustment of control R1, the IF power level should be able to be limited to the nominal level of -6 dBm. Vary the RF power between -50 and -30 dBm and observe a constant IF power level of -6 dBm. Next, disconnect the RF signal generator and place a jumper across resistor R25. Connect a voltmeter to TP1. The DC offset control R20 should now be adjusted for 0 VDC on the voltmeter. Using a spectrum analyzer and an RF pickup loop, the VTO output is monitored. Input Pin 3 XTAL OSC INHIBIT is tied to +12 volts and R36 is adjusted to set the VTO operating frequency at 300 MHz. Then with PIN 3 grounded, the RF pickup loop is used to monitor the XTAL oscillator output. L8 is adjusted to peak up the oscillator output power. This completes the proper alignment of the demodulator board.

These alignments are only preliminary as all adjustments will have to be re-optimized when the demodulator board is matched to its IF filter and UHF tuner in the final indoor unit assembly.

3.6 CHANNEL SELECT LOGIC AND POWER SUPPLY SUBASSEMBLY

3.6.1 Functional Description

The channel select logic and the power supply are on the same printed circuit board. The schematic is shown in Figure 3-16 and the assembly of the board is shown in Figure 3-17. These two board functions are described individually.

The power supply converts the single phase 115 VAC voltage to ±12V regulated for the indoor unit power requirements and unregulated ±20V for the outdoor unit power requirements. The ac input line is filtered by metal oxide varistors for equipment protection against failures caused by transient voltage spikes. The varistor impedance changes from a very high standby value to a very low conducting value when exposed

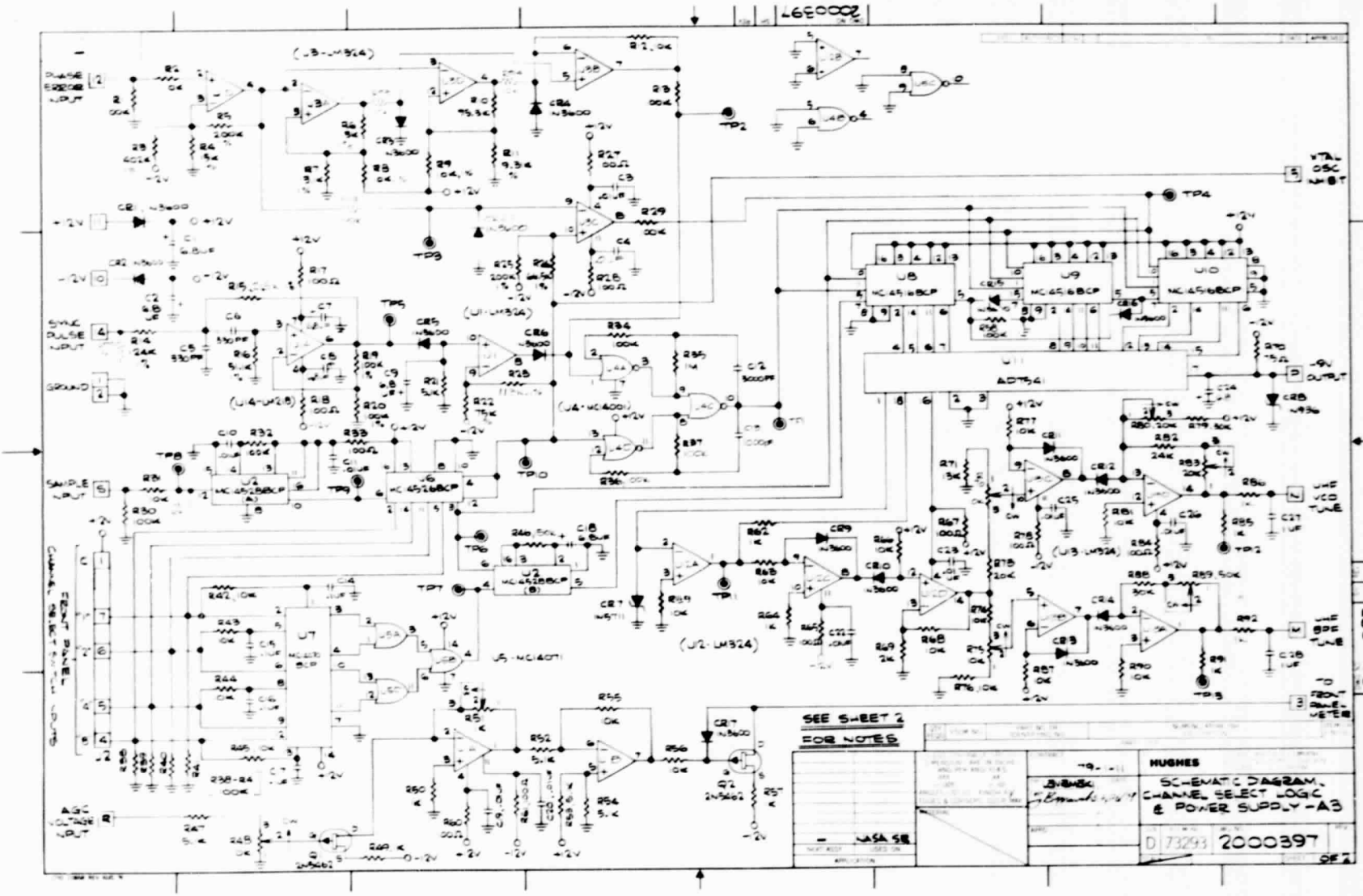


Figure 3-16A Channel select logic and power supply board, schematic.

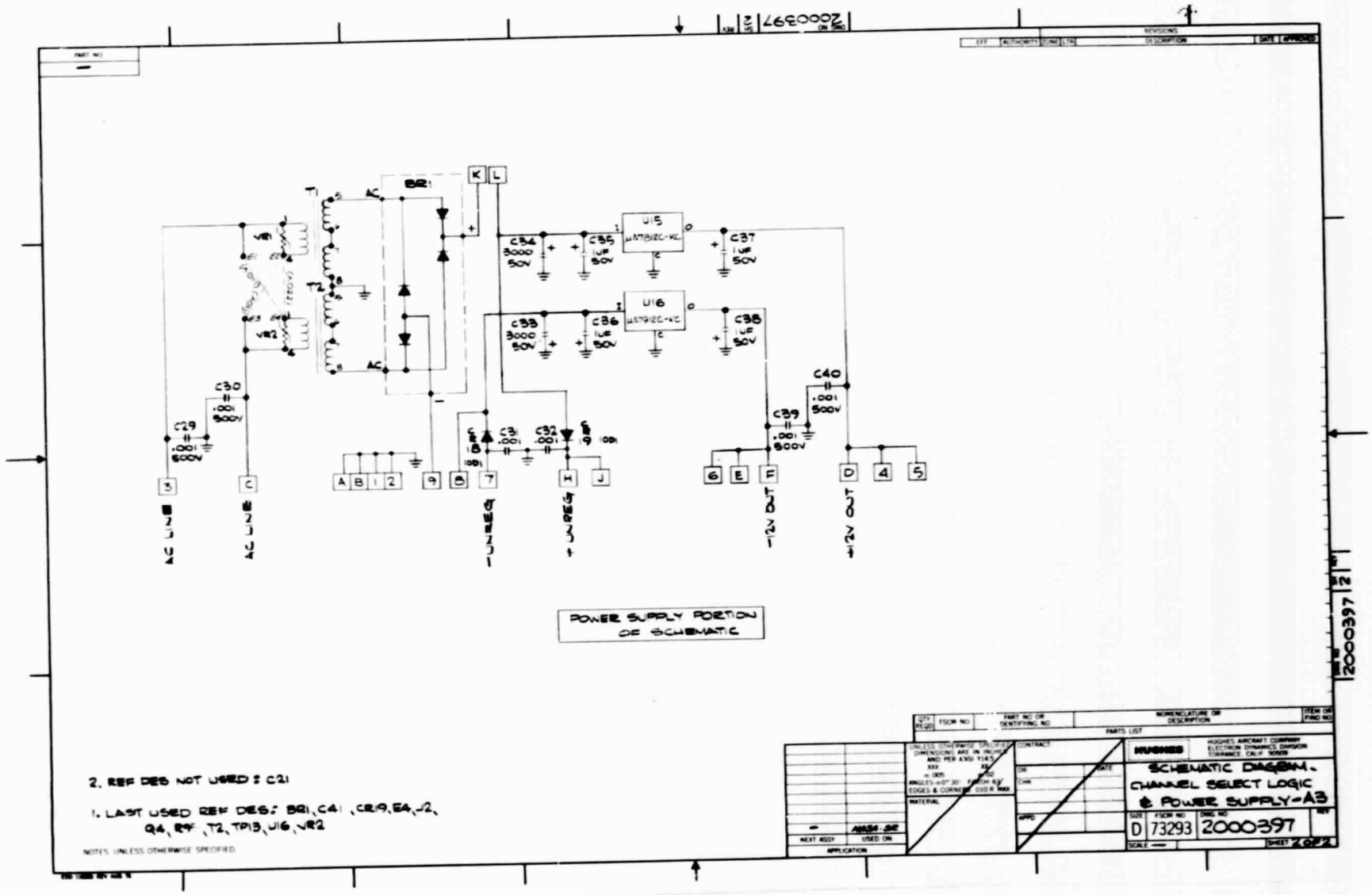


Figure 3-16B Channel select logic and power supply board, schematic.

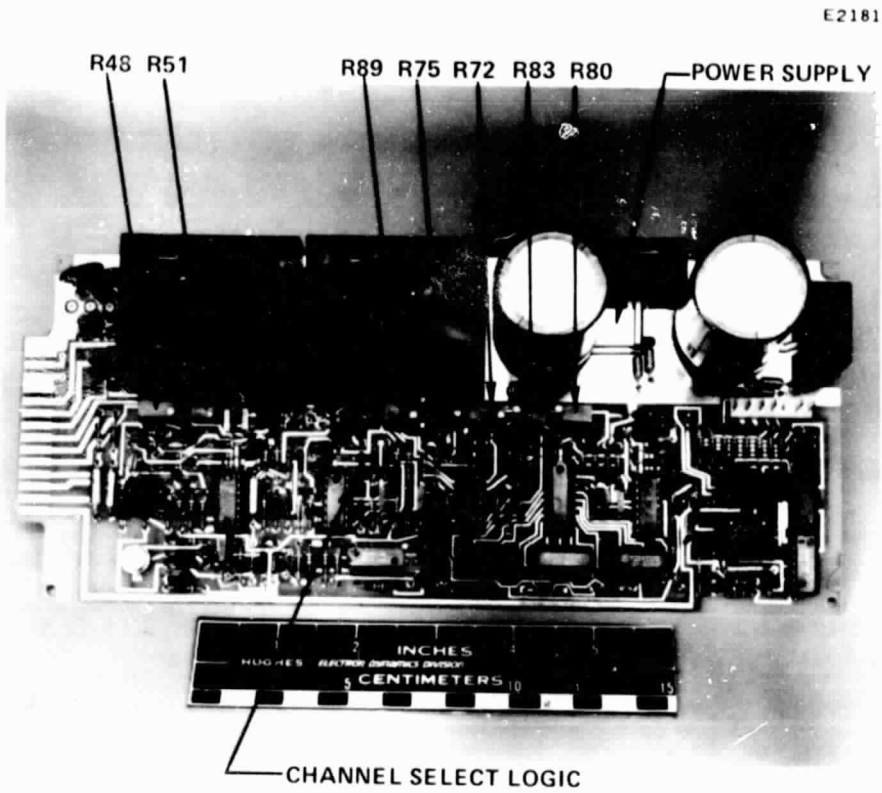


Figure 3-17 Channel select logic and power supply board.

to high energy voltage transients. Thus, with the fast varistor response time (< 50 nsec), the transient incoming voltage is changed to a safe level.

The power transformers can be wired for 110V or 220V AC operation. The outputs of the voltage transformers are directed to the full wave rectifying bridge whose output is the unregulated ±20 volts. This voltage is directed through protection diodes to the unregulated voltage output pins leading to the outdoor unit. The unregulated voltage is also directed through the power supply filter capacitors and the ±12 volts integrated circuit voltage regulators supplying power to the indoor unit subassemblies.

The channel select logic performs the function of sensing the video channel selected by the front panel switches and tuning the microstrip tuner band pass filter and voltage controlled oscillator for reception of the proper video channel. This tuning scheme utilizes low cost CMOS logic and eliminates the need for multiplexing the voltages from individually adjusted potentiometers for each channel. Because the tuning method operates as a closed loop system, continuously monitoring the demodulated signal output, an automatic tuning voltage correction takes place, compensating for any offset frequencies and any inherent temperature drifts occuring at the outdoor Gunn local oscillator or at the UHF microstrip VCO. This action ensures that the phase lock loop demodulator operates at optimum conditions at all times.

The tuning action takes place by sweeping the UHF VCO and counting the output pulses from the sample circuit on the demodulator board. When a video channel is selected or at power turn on, a voltage transient tirggers a one shot whose output pulse resets the control logic. The reset pulse is observed at TP6 and is typically 0.4 sec in duration, long enough for any switch contact bounce to have settled. During reset the digital channel code is loaded into the pulse count register of the

pulse counter, U6. The channel code is such that selection of channel one loads the number 12 in the pulse count register, channel two loads the number 11, channel three loads 10, etc. This code accommodates the sweep of the UHF microstrip VCO which is from 1750 MHz to 1250 MHz. During reset the DAC counters, U8, U9, and U10, are set to their start state.

At the end of the reset pulse, the UHF VCO sweep mode begins. The fast clock, U4D & C, with f ≈ 4.0 KHz, decrements the DAC counters. This action causes the output of the DAC amplifier, U12A, at TP11 to have a ramp voltage going from +9 volts to zero. This ramp voltage is sent through a voltage shaper U13C, D whose output at TP12 acts to linearize the sweep of the UHF VCO. A similar voltage shaper U13A, B is used to derive the tuning voltage for the UHF BPF. The adjustment of the two potentiometers R75, R89 will allow the BPF to track the VCO in unison.

In the sweep mode, the UHF VCO sweeps from 1750 MHz to 1250 MHz. The low pass filter VCO sample output at J2 of the microstrip board has a steep cutoff at 1740 MHz. This provides a reference point for the sweep so that VCO frequencies above 1740 MHz do not affect the tuning circuitry. The VCO sample output is mixed with a harmonic of the 40 MHz oscillator on the Demodulator Board, resulting in a sample output pulse from the Demodulator Board whenever the UHF VCO sweeps past a 40 MHz harmonic. During this sweep mode TP10 is low and the 300 MHz VTO on the Demodulator Board is turned off.

The sample pulse is received by the channel select logic and triggers a one shot. The output pulse from the one shot is counted by the pulse counter U6. When the selected count has been reached, the proper video channel selected has been received and TP10 goes high. This turns off the fast clock, turns off the 40 MHz crystal oscillator on the Demodulator Board, turns on the 300 MHz VTO on the Demodulator Board, and forces TP2 high so that the logic clock is disabled. If the channel

selected has video present, the sync pulse input is detected and enables the slow clock control by the comparators U3A, B and D. The 15.75 KHz active filter at the sync pulse input ensures that only the sync pulse presence enables the slow clock.

With the received video signal demodulated by the phase lock loop demodulator on the Demodulator board, the DC phase detector error voltage is a function of the frequency offsets occurring from the UHF VCO and from the 10.75 GHz LO in the outdoor downconverter. When the DC phase error is greater than +0.05 volt TP2 goes low turning on the slow logic clock, U4 A & C and TP4 goes low. This action decrements the voltage applied to tune the UHF VCO and decreases the DC phase error. When the error decreases to less than 0.005 volt TP2 goes high and the logic clock goes off. This automatic nulling of the phase detector dc error ensures the optimum phase lock demodulator performance. Similar action occurs when the phase detector dc error is greater in magnitude than -0.050 volts. This closed loop tuning operation means that the local oscillator in the outdoor downconverter and in the microstrip tuner can have relaxed tolerances on their output frequencies.

For the present application with the downconverter LO and RF frequencies specified at 10.75 GHz and 12.08 GHz, respectively, the selected channel for video reception is channel 10.

When the tuning condition occurs that the selected channel does not have video present, TP2 is forced high and holds the clock off so that any invalid dc phase detector error does not activate the DAC counters.

A timing diagram showing the channel select logic action is shown in Figure 3-18. The diagram is for the case that channel ten is selected and video is present on channel 10.

The channel select logic board also contains a nonlinear amplifier which adjusts the monitored IF AGC voltage level before driving the signal

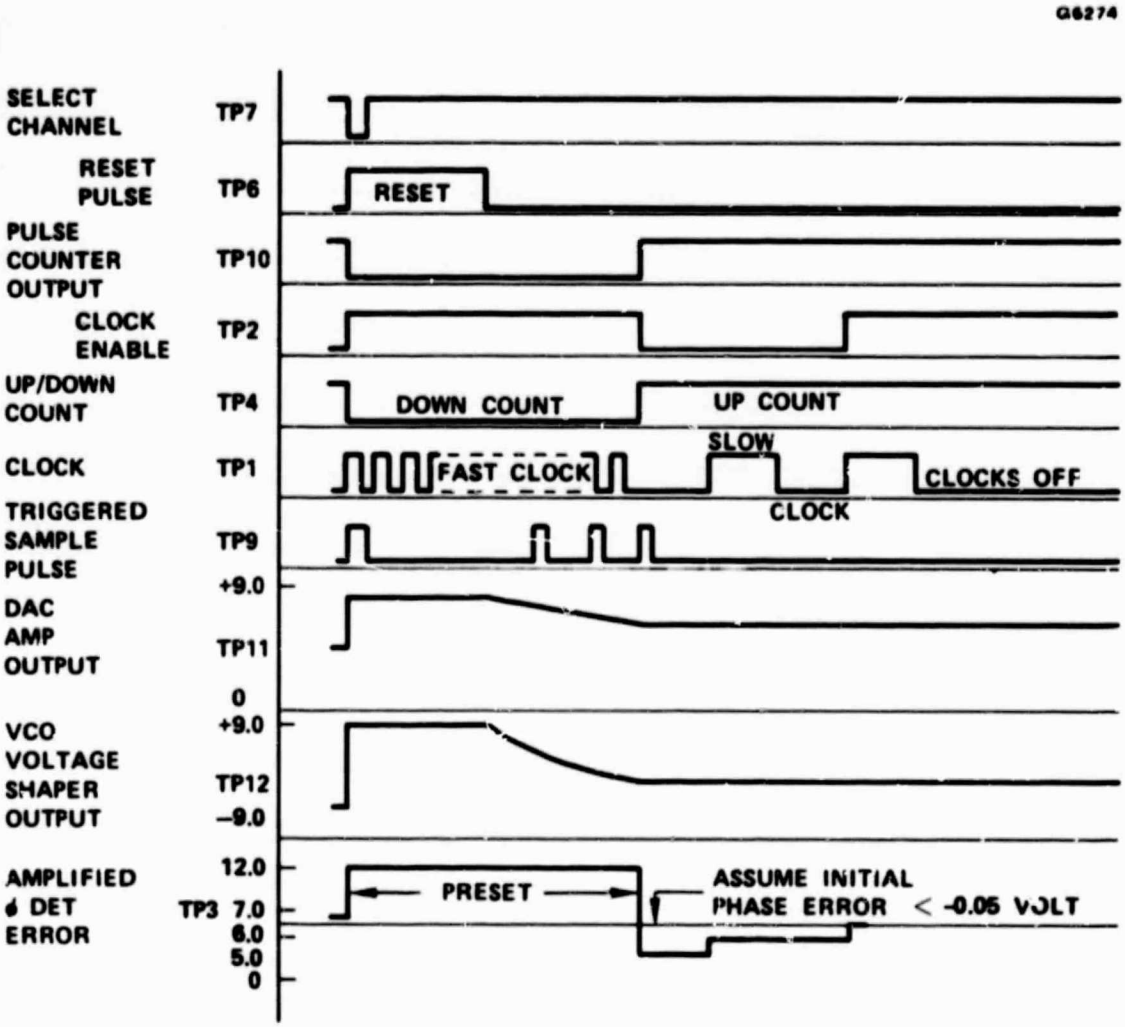


Figure 3-18 Channel select logic, timing diagram. Example: channel 10 selected with video present.

strength panel meter. The adjustment of two potentiometers allows proper adjustment of the metering circuit for the operating AGC voltage range.

3.6.2 Alignment and Test

To evaluate the two board functions on each assembled Channel Select Logic and Power Supply board, the board will be placed in a test fixture which will include a Demodulator board, a UHF tuner, an Indoor IF Amplifier and a Signal Processor board to allow proper evaluation of the control circuit functions.

The Power Supply is evaluated by inputting the ac line voltage to the board and observing the voltage outputs. The voltage outputs are loaded with fixed resistive loads which draw 150% more current than the nominal power supply operating currents. The ±12 volt outputs are loaded with 33Ω. The unregulated ±20 volts outputs are loaded with 100Ω. The test technician will verify that the ±12 outputs are within ±0.50 volts and that the unregulated outputs are within 18 to 20 volts including voltage ripple.

The evaluation of the channel select logic involves a specific sequence of tests to verify proper operation of all the circuits on board. The logic reset pulses at TP6 and 7 are monitored as the different channels are selected by the channel select switches. The pulse durtion at TP7 is verified to be greater than 0.5 ms and the pulse duration at TP6 is verified to be 0.4 sec ±0.2 sec. At this time, it is also observed that the logic clock output at TP1 is operating at a nominal 4.0 KHz rate

The active filter output at TP5 is evaluated by applying the Sync Pulse signal from the Signal Processor board. The Sync Pulse signal is derived from the composite Video signal input to the Signal Processor board. With the Composite Video signal "ON" the active filter will respond

to the 15.75 KHz content of the Sync Pulse and a 15.75 KHz sine wave at a level of 4.0 ±1.0 volts peak will appear at TP5. With the Composite Video signal "OFF" the Sync Pulse signal will be broadband noise and the output of the active filter at TP5 will be less than 0.5 volt peak.

The UHF VCO voltage shaper is evaluated by inputting +12 V on all channel select switch inputs. This allows the DAC amplifier output, at TP11, to produce a repetitive triangular wave shape varying from +9 volts to 0 volts. Three pots in the UHF VCO voltage shaper network are adjusted while monitoring TP9, the sample pulse one-shot output, and TP12, the voltage shaper output. R72 controls the nonlinearity factor in the voltage sweep whereas R83 and R80 control the voltage shaper gain and offset voltage.

When the VCO tune voltage is adjusted to sweep between ±10 volts, the UHF VCO will be sweeping between 1200 and 1800 MHz. This will cause the sample pulses from the Demodulator board to trigger pulses at TP9. The nonlinearity of the tune voltage is adjusted to make the series of pulses observed at TP9 to be equally spaced from each other. This condition shows that the VCO sweep has been essentially linearized. With the channel select switches engaged again, the channel tuning function of the logic board is evaluated. For this evaluation the RF input to the UHF tuner consists of an RF carrier modulated by the composite video test signal, with the RF carrier freqency selectable for each of the twelve video channels. When a channel is selected, say channel N, it is observed that 13-N pulses appear at TP9. At the end of these 13-N pulses, TP10 goes high to +12 volts. That is, the pulse counter has timed out. At this time the amplified dc phase error from the Demodulator board is engaged and observed at TP3. With TP10 going high the fast clock turns off, and the slow clock is engaged to null out the dc phase error and drive the voltage level at TP3 to a nominal +6 volts. As the RF carrier to the UHF tuner is varied, the voltage at TP3 will

change. When this voltage becomes less than 5 volts or greater than 7 volts the slow clock is engaged, driving the voltage back to 6 volts. Now, with the video modulation turned "OFF", TP2 is observed to go to +12 V, disengaging the slow clock.

The voltage shaper supplying the UHF BPF tune voltage is next adjusted to allow the BPF to track the UHF VCO in frequency. For this alignment, a wideband noise signal is applied to the UHF tuner RF input, J1, and the UHF tuner at TP1 is monitored on a spectrum analyzer. In the voltage shaper network R75 controls the voltage nonlinearity and R89 controls the voltage shaper gain. For a voltage sweep adjusted for 0 to +11 volts, the voltage nonlinearity is adjusted to give a BPF response, as observed on the spectrum analyzer, which is centered at the correct frequency for each video channel selected.

With all the above alignment and test procedures completed, there remains the evaluation of the AGC metering circuits. This is evaluated by varying the IF power input to the IF amplifier board. The closed loop AGC action through the AGC amplifier on the Demodulator board will drive the AGC voltage applied to U1 on the IF amplifier board to the level necessary to maintain a constant IF power input to the Demodulator board. By adjustment of R48 and R51 on the Logic board the AGC voltage will drive the Signal Strength meter indication to a level representative of the IF amplifier input power.

With R48 turned fully counterclockwise, R51 is adjusted to give a full scale meter deflection. Then with the IF amplifier input power at a level of -55 dBm R48 is adjusted to give a minimum meter deflection. Finally, with the IF amplifier input at -30 dBm, R51 is adjusted to give a full scale meter deflection. In the assembled receiver the meter deflection is indicative of the RF power received at the outdoor unit waveguide input.

Presently, on the Logic board, three potentiometers are used for adjustment of the UHF VCO tuning voltage and two potentiometers are used for adjustment of the UHF BPF tuning voltage. It is felt that during production these five potentiometers may possibly be replaced by fixed resistors as it is projected that the required tuning voltage for the VCO and BPF will be quite similar for each UHF tuner board on a unit to unit basis.

The channel select tuning operation is flexible enough so as not to require ideal linear tuning of the VCO and BPF. However, the potentiometers are included to provide an additional alignment flexibility until the UHF tuner performance has been evaluated over a number of receivers assembled.

3.7 ASSEMBLED INDOOR UNIT ALIGNMENT AND TEST

The final indoor unit alignment and test will be accomplished with the circuit boards assembled into the deliverable chassis. With each board aligned and tested prior to final assembly, the final alignment will require a minimal of time and the final test will follow the acceptance test listed in Appendix B.

The final alignment will require optimization of the controls on the Demodulator board and the Channel Select Logic and Power Supply board. The AGC level control and the phase lock loop controls on the Demodulator board must be adjusted to accommodate the particular UHF tuner and IF Amplifier subassemblies used in the final assembly. Optimization of these controls will ensure optimum phase lock loop performance and will result in an onset of perceptible impulse noise in the video picture at a carrier to noise ratio below 9 dB. The metering circuit on the Logic board must be reoptimized to accommodate the particular IF amplifier subassembly installed in the final receiver. The alignment procedure for the metering circuit follows that for the initial board

alignment. Alignment of the voltage shapers for the UHF VCO and the UHF BPF is not expected to be repeated in the final assembly due to the expected repeatable performance to be obtained from the UHF Tuner board on a unit to unit basis.

The final test of the indoor unit will verify that all system performance factors are within specification. The acceptance test to be followed is as listed in Appendix B and will verify the proper RF, video, and audio response. The estimated time to complete the final test of the complete indoor unit assembly is 0.6 hours per unit for the 1000 unit production lot.

4.0 PRODUCTION — MATERIAL COST BREAKDOWN FOR LOTS OF 10, 100 AND 1000.

A detailed pricing analysis for this prototype receiver has been conducted to determine the estimated cost for each receiver in production quantities of 10, 100, and 1000 receivers. The most important cost consideration in the receiver is the low noise GaAs FET amplifier. Hughes has made a commitment to develop low cost 0.5 micron gate length FET devices in production quantities. The production devices are unpackaged chips with a nominal noise figure of 3.0 dB with associated gain of 9.0 dB at 12 GHz. The low noise amplifier includes three FET amplifier stages and a bandpass filter. The projected costs of the 11.7 - 12.2 GHz GaAs FET amplifier is presented in Table 4-1.

TABLE 4-1

MANUFACTURING COSTS OF 11.7-12.2 GHz AMPLIFIERS FOR LOW COST EARTH TERMINALS

Year	Quantity	FETs (quant.-3)		Materials & Labor $(2)	Total $ per Ampl.(1)
		$/Each	$/Sub-total		
1978	10	185	555	743	1298
1981	10	50	150	935	1085
1978	100	126	378	358	736
1981	100	35	105	451	556
1978	1000	111	333	209	542
1981	1000	30	90	263	353

(1) Total cost includes Materials + Labor + Labor Burden (152%). Includes 3 FETs, 3 amplifier stages and filter.

(2) Assumes 8% per year inflation, 3 years.

All costs for the receiver have been broken down for the mechanical and electrical components for the subassemblies in the outdoor and the indoor units. The electrical components include all resistors, capacitors, transistors, integrated circuits, all other electronic components and printed circuit board. The mechanical components include all chassis, covers, cans shields, brackets, and all mounting hardware. The material cost breakdown for the indoor and outdoor unit is presented in Table 4-2.

The pricing information shown in this table is representative of the prototype receiver delivered at the end of this program. The electronic component pricing is based on purchases in contract quantities or in economic lot quantities for the 1000 unit contract. All mechanical parts are purchased from outside vendors. Chassis covers, and cabinetry are purchased from outside vendors already formed, pierced, tapped, semi-assembled, painted, and silk-screened. For the indoor unit, all mechanical parts are either stamped sheet metal or injection molded plastic. For the outdoor unit, the chassis are milled out for the 10 unit contract and casted in a rubber-plaster mold for the 100 unit and 1000 unit contracts.

For the existing prototype the projected cost per unit is much higher than desired for the 1000 lot quantities. This is because of the high price for the GaAs FET amplifier as well as a less than optimum prototype design in terms of parts count and circuit function.

The FET device cost can quite likely become a lower cost item with the maturing technology. Though our projections are based on Hughes current GaAs FET capability and on Hughes in-house development programs, significant breakthroughs in the technology may result in significant price reductions.

Several currently available GaAs FET devices are listed in Table 4-3. A device such as the Plessey GAT-6 has a specified noise figure of 2.2 dB at 12 GHz with associated device gain of 9.5 dB.

TABLE 4-2

PRODUCTION RECEIVER MATERIAL COST BREAKDOWN
FOR LOTS OF 10, 100 AND 1000

	10 Units	100 Units	1000 Units
Indoor Unit			
Chassis, Electrical	91.56	73.25	58.60
Chassis, Mechanical	311.00	34.26(2)	34.26(1)
Channel Select Logic and Power Supply Board	87.72	70.18	56.14
Signal Processor Board	59.16	47.33	37.86
Demodulator Board	118.75	95.00	76.00
Microstrip Tuner Board	117.03	93.63	74.90
IF Amplifier Board	57.82	46.25	37.00
	843.04	459.90	374.76
Cables and Connectors	18.90	15.00	12.00
Outdoor Unit			
Chassis, Electrical	139.69	111.75	89.40
Chassis, Mechanical	379.00(5)	95.84(4)	55.81(3)
FET Amplifier and BPF(6)	1298.00	736.00	542.00
Mixer	23.44	18.75	15.00
Gunn L.O.	15.63	12.50	10.00
IF Amplifier Board	29.78	23.83	19.06
Power Supply Board	10.08	8.06	6.45
	1895.62	1006.73	737.72
Total Material Cost			
Prototype	2757.56	1481.63	1114.48

(1) Does not include $9,000.00 tooling for stamping dies.

(2) Does not include $9,000.00 tooling for stamping dies.

(3) Does not include $12,000 tooling cost for casting dies and injection molds.

(4) Does not include $5,650 tooling cost for casting dies and injection molds.

(5) All chassis tape machined.

(6) Total cost per amplifier based on GaAs FET amplifier and BPF cost unit projection for 1978.

TABLE 4-3

COMMERCIALLY AVAILABLE LOW NOISE FETs
(NOVEMBER 20, 1978)

Manufacturer	Device	12 GHz Noise Figure*	12 GHz Assoc. Gain*	(1-10) Cost
Dexcel	2503	3.1 dB	8.0 dB	$ 65
N.E.C.	24400	3.3 dB	8.5 dB	75
	28800	3.0 dB	9.0 dB	125
Plessey	GAT-5	2.9 dB	11.0 dB	105
	GAT-6	2.2 dB	9.5 dB	185
Varian	VSX-9305	2.8 dB	11.0 dB	95

*Manufacturers data for chip devices.

This device may make it feasible to relax our design parameters to result in a much lower cost receiver (provided, of course, that the FET device significantly reduces in price). We may conceiveably eliminate the die casted waveguide circulator and load and use a less expensive microstrip isolator with a higher insertion loss without increasing the noise figure above 4.0 dB. With the higher FET device gain, the noise figure requirements for the mixer and IF amplifier is much relaxed and may result in savings in component cost and testing time. Assuming that a device similar to the GAT-6 is available in 1981 at $30/unit in 1000 lot quantities, we may expect to save $50 component cost by use of the microstrop isolator and the less critical mixer and IF amplifier components.

The prototype outdoor downconverter can also be further simplified and reduced in size by the use of an integrated type of converter in one mechanical housing. The isolator, GaAs FET amplifier, bandpass filter, mixer and local oscillator can all be combined as a fully integrated microwave front end. The IF amplifier would remain the same as the

present prototype which, though it is large in size, is very low in cost. The integrated converter would take advantage of GaAs FET technology developments not yet refined for practical application. The optimum integrated converter would use monolithic microwave analog IC concepts. The GaAs monolithic microwave technology is a technological step in the early developmental stage and can offer many advantages over the present microwave integrated circuit (MIC) technology. The monolithic receiver front end would have the circuit elements and active elements grown right in the GaAs substrate. This monolithic approach would result in lumped circuit elements due to the small sizes involved and would result in a receiver front end which requires a minimum of hand labor to assemble or tune. The expected size of this downconverter unit would be on the order of 75 mm (W) x 150 mm (L) x 75 mm (H) including monolithic front end waveguide adapter, power supply regulator, IF amplifier, and interface connectors. This downconverter would be a more cost effective approach when the quantity of receivers required is greater than 100,000 units. This approach would use state of the art designs and would incur the largest development costs, but would result in a lower receiver sale price.

The prototype design can also be further refined to result in significant material cost savings. Because the commercial customer such as the in-house customer is not at all interested in the signal strength level, the meter can be eliminated. Similarly, a simpler switch such as a properly coded thumbwheel switch can be used rather than the interlocked bank of switches presently used. This change would also eliminate the switch board along with much mechanical mounting hardware. Many other changes are possible to use less expensive electronic devices by modifying the various electronic circuits. The present design calls for many discrete components on the tuning logic board, including CMOS counters, op-amps, and many resistors. The parts count and assembly of this board would be greatly improved if much of this circuit was integrated on a single integrated circuit. The design of this I.C. would be justifiable if the quantity of receivers required were greater than 100,000 units.

It is reasonable to assume that with the design changes just discussed the receiver cost can be lowered significantly and result in a price much lower than $1,000. However, these developments are justified only when the quantity of receivers required exceeds 100,000 units.

The prototype design developed under the present contract is limited in scope and is consistent with the quantity requirements of 1000 unit lots. Many of the state of the art design approaches could not be taken advantage of for the present requirements.

It must be emphasized that the intended use of the 12 GHz satellite receiver is for the commerical satellite system anticipated in the 1980's which can create a market for over 1,000,000 units. With this is mind, the integrated satellite receiver is the next developmental step which must undergo development today.

5.0 PRODUCTION — LABOR BREAKDOWN FOR LOTS OF 10, 100, AND 1000

The labor costs for assembly and inspection per receiver manufactured are listed in Table 5-1. Fabrication costs for housings, printed-circuit boards, and substrates are included in the materials costs since these items are purchased outside. This estimate is based on current production of similar hardware.

The direct labor rates used in this estimate are rates currently paid to personnel assigned to our Microwave Communications Products activity, which will be given responsbility for future production of this product. The overhead rate used is the Government-approved Division-wide bidding rate.

The manufacturing techniques for the 10 unit and 100 unit contracts will be those used in low-volume production. The 1000 unit contract will allow the use of more cost-efficient scheduling, methods, tooling, and equipment. Discrete components will be cut and formed on semiauto-matic machines. After assembly, circuit boards will be wave-soldered. An automatic wire cut and strip machine will be used to form interconnecting wires. Printed circuit boards will be assembled in lot sizes chosen to minimize labor input and handling.

The FET amplifier stages and the BPF are microwave integrated circuits photolithographically etched on alumina substrates which are then soldered on to Kovar carriers. The process and assembly techniques for manufacturing microwave integrated circuits at Hughes Electron Dynamics Division result in low cost, high yield and high reliability. All other printed circuit boards have their components attached by belt soldering. Except for the microstrip components, all components are soldered in one pass through the machine which yields stress free component solder joints.

TABLE 5-1

PRODUCTION RECEIVER - LABOR BREAKDOWN FOR LOTS OF 10, 100, AND 1000

	10 Units						100 Units						1000 Units					
	Assembly		Inspection		Test		Assembly		Inspection		Test		Assembly		Inspection		Test	
	Hrs	Cost	Hrs	Cost	Hrs	Cost	Hrs	Cost	Hrs	Cost	Prs	Cost	Hrs	Cost $10/Hr	Hrs	Cost $18.2/ Hr.	Hrs	Cost $16.4/ Hr.
Indoor Unit Assembly(1)	11.3	$113.00	1.66	$30.20	5.14	$ 84.30	5.3	$ 53.00	0.78	$14.20	1.43	$ 23.45	3.4	$ 34.00	0.5	$ 9.10	0.6	$ 9.84
Channel Select Logic and Power Supply	5.3	53.00	0.66	12.01	4.42	72.49	2.5	25.00	0.30	5.46	1.44	23.62	1.6	16.00	0.2	3.64	0.45	7.38
Signal Processor Board	4.00	40.00	1.00	18.20	7.36	120.70	1.87	18.70	0.46	8.37	2.4	39.36	1.2	12.00	0.3	5.46	0.75	12.30
Demodulator Board	2.00	20.00	0.50	9.10	4.90	80.36	0.94	9.40	0.23	4.18	1.6	26.24	0.6	6.00	0.15	2.73	0.50	8.20
Microstrip Board	9.3	93.00	1.16	21.10	4.9	80.36	4.36	43.60	0.54	9.83	1.6	26.24	2.8	28.00	0.35	6.37	0.50	8.20
IF Amplifier Board	1.1	11.00	0.15	2.73	1.97	32.30	0.78	7.80	0.10	1.82	0.64	10.49	0.5	5.00	0.05	0.91	0.20	3.28
Total, Indoor Unit	33.00	$330.00	5.13	$93.34	28.69	$470.51	15.75	$157.50	2.41	$43.86	9.11	$149.40	10.10	$101.00	1.55	$28.21	3.00	$49.20
Outdoor Unit Assembly(1)	5.0	50.00	1.00	18.20	4.90	80.36	2.34	23.40	0.46	8.37	1.60	26.24	1.5	15.00	0.3	5.46	0.5	8.20
FET Amp. & BPF(2)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Mixer	1.0	10.00	0.20	3.64	1.97	32.30	0.47	4.70	0.15	2.73	0.64	10.49	0.30	3.00	0.1	1.82	0.20	3.28
Gunn LO	0.8	8.00	0.15	2.73	3.24	53.14	0.40	4.00	0.10	1.82	1.00	16.40	0.25	2.50	0.05	0.91	0.33	5.41
IF Amplifier	2.5	25.00	0.20	3.64	4.2	68.88	1.17	11.70	0.15	2.73	1.36	22.30	0.75	7.50	0.1	1.82	0.37	6.07
Power Supply Board	0.66	6.60	0.15	2.73	0.49	8.04	0.3	3.00	0.1	1.82	0.16	2.62	0.2	2.00	0.05	0.91	0.05	0.82
Total, Outdoor Unit	9.96	$ 99.60	1.70	$30.94	14.80	$242.72	4.68	$ 46.80	0.96	$17.47	4.76	$ 78.05	3.00	$ 30.00	0.60	$10.92	1.45	$23.78
Total Receiver	42.96	$429.60	6.83	$124.28	43.49	$713.23	20.43	$204.30	3.37	$61.33	13.87	$227.45	13.10	$131.00	2.15	$39.13	4.45	$72.99
Total Labor Hrs	93.28 Hours						37.67 Hours						19.70 Hours					
Cost Includes assembly, inspection, alignment and tuning and final test labor	$1,267.11						$493.09						$243.11					

(1) Assembly test time is the time to perform final receiver acceptance tests.

(2) The labor and material cost for the FET amplifier and BPF was broken down separately in Table 4.2, the total cost was included in Table 4.3.

The production costs of the various subassemblies is based on hand insertion of components as presently performed at Hughes Microwave Communications Products. We are expecting to implement automatic insertion techniques in the 1000 lot quantities and this should result in significant labor cost savings.

6.0 ESTIMATED COST FOR EACH RECEIVER IN PRODUCTION QUANTITIES OF 10, 100 AND 1000 RECEIVERS

The following Table 6-1 is the summary of the projected production costs of the receiver. These figures are based on the prototype receiver developed at Hughes and based on Hughes current experience in manufacturing and testing satellite video receivers and microwave video links. The costs include overhead but do not include profit or tooling costs.

TABLE 6-1

COST SUMMARY

	10 Units	100 Units	1000 Units
Materials and Component Costs	$2757.56	$1481.63	$1114.48
Assembly and Inspection Labor	553.88	265.63	170.13
Alignment, tuning, and test labor	713.23	227.45	72.98
Total Manufacturing Cost	4024.67	1974.71	1357.59
G&A @ 13.3%	535.28	262.64	180.56
Total Estimated Cost	4559.95	2237.35	1538.15

C-2

These costs reflect the present capabilities at Hughes Microwave Communication Products and does not reflect the use of automatic insertion techniques or the use of any of the cost saving design changes discussed earlier.

7.0 ADAPTABILITY TO FIELD REPAIR AND LABORATORY REPAIR

The protogype 12 GHz receiver will provide ease of repair and adaptibility to technology changes. The indoor and outdoor units are constructed on modular subassemblies attached to a mainframe. Since all subassemblies are identical on a unit to unit basis, a receiver failure may be serviced by locating the subassembly which failed and replacing with a new subassembly. The failed subassembly may then be repaired in a repair facility. An alignment procedure will be followed when replacing any of the printed circuit boards in the outdoor or indoor units. Because of the critical nature of X-band circuitry, no field repair will be attempted on the FET Amplifier and BPF, the X-Band mixer, or the Gunn local oscillator. If any of these subassemblies are faulty the entire outdoor unit will be replaced and the defective unit returned for labortary repair.

Outdoor Unit

Field servicing the outdoor unit will consist of locating the fault at either the power supply board or IF amplifier, or at the X-band subassemblies. It the power suply board or IF amplifier board is faulty, field replacement with a working subassembly will bring the outdoor unit to a working status. The faulty board can then either be repaired at a repair facility or sent back to the factory for laboratory repair.

Factory laboratory repair will always be required for a faulty X-band subasembly. In the laboratory, a visual check will determine if there is any physical damage.

The faulty X-Band subassembly will be determined by removing the subassemblies from the housing and substituting good units.

Removal will be achieved by unplugging dc connections, unsoldering microwave connections, and removing subassembly clamps. Once the faulty subassembly is replaced the outdoor unit will be ready to go back into the field.

Indoor Unit

Field servicing of the indoor unit will consist of isolating the fault to a particular circuit board and replacing that board. Each board will have readily accessible test points which will give sufficient information to isolate the fault. The boards will have plug-in dc connections and coax connectors where appropriate. The boards are held to the chassis with a minimum number of screws to make board removal easy within a minimal of time.

On the UHF tuner board the parameters mointored are the BPF tune voltage, the VCO tune voltage, and power supply voltage. On the IF circuit board the test points are AGC voltage, and power supply. The test points on the Demodulator Board are AGC voltage, VCO tuning voltage, DC phase error voltage and power supply. The Signal Processor Board test points are the video amplifier bias levels, the audio phase lock demodulator bias and tuning voltages and the clamping circuit bias levels. The Channel Select Logic Board provides test points for the one shot outputs, the pulse counter output, the clock, the input and output levels for all comparators, and the voltage at various points in the tuning voltage network. These test-points provide sufficient information to quickly isolate most faults to a particular board. With the replacement of a particular board, an alignment procedure will be followed. The factory will provide fault diagnosis information for systematic location and repair of faults once the board is connected to the appropriate test equipment. Since each board contains a number of independent circuit functions, repair will not be difficult and will therefore be inexpensive.

Due to the flexible design of the prototype receiver, the receiver is quite readily adaptable to changes in RF transponder center frequency and in improvements in the state of the art. Changes in the RF channel center frequency is accomodated by changing the frequency of oscillation of the crystal oscillator on the demodulator baord. As the state of the art in GaAs FET transistors improves, the FET amplifier can readily accommodate the new transistors.

8.0 NEW TECHNOLOGY CLAUSE

The work involved in developing this prototype receiver did not involve the development of any new technology but stems from the accomplishments at Hughes in the field of earth station receivers for video transmission by satellite. The phase lock demodulation techniques discussed in this report are presently in use in the 4 GHz satellite receiver product line that the Electron Dynamics Division is currently offering for commercial sale. The phase lock demodulator is in itself a patented technique developed earlier (U.S. patent numbers 3, 611, 168 and 3, 346, 850).

APPENDIX A

DETAILED ANALYSES AND CALCULATIONS OF 12 GHz SATELLITE RECEIVER PERFORMANCE

PHASE DETECTOR

If it is assumed that the discriminator is a balanced phase detector composed of peak-detecting diodes, the discriminator output voltage can be derived from the vector diagram in Figure 1. For sinusodial variations with time, the synchronizing signal e_1 and the reference signal e_2 can be written as:

$$e_1 = E_1 \cos \phi_1 \qquad (C1)$$

and

$$e_2 = E_2 \sin \phi_2 \qquad (C2)$$

where ϕ_1 and ϕ_2 are functions of time and for reasons of simplicity in the later developments, it is arbitrarily assumed that ϕ_1 and ϕ_2 are in quadrature when the system is perfectly synchronized, that is when $\phi_1 = \phi_2$.

While one of the discriminator diodes is fed with the sum of e_1 and $e_2/2$, the other is fed with the difference of these two vectors. The resulting rectified voltages Ed_1 and Ed_2 can be established by simple trigometric relations. Defining a difference phase $\phi = \phi_1 - \phi_2$, one obtains

$$Ed_1^2 = E_1^2 + \frac{E_2^2}{4} + E_1 E_2 \sin \phi \qquad (C3)$$

and

$$Ed_2^2 = E_1^2 + \frac{E_2^2}{4} - E_1 E_2 \sin \phi \qquad (C4)$$

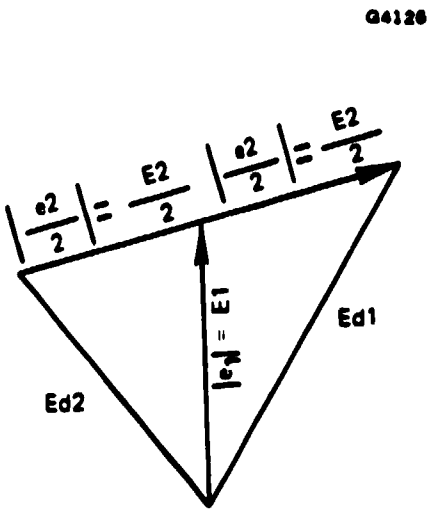


Figure 1 Discriminator vector diagram.

The discriminator output voltage Ed is equal to the difference of the two rectified voltages so that

$$ed = Ed_1 - Ed_2 = \frac{2E_1E_2}{Ed_1+Ed_2} \sin \phi \qquad (C5)$$

If the amplitude E_1 of the synchronizing signal is larger than the amplitude E_2 of the reference signal, one obtains

$$Ed_1 + Ed_2 \approx 2E_1 \qquad (C6)$$

The discriminator output voltage than becomes

$$ed = E2 \sin \phi \qquad (C7)$$

and is independent of the amplitude E_1 of the synchronizing signal. As ϕ_1 and ϕ_2 are time-varying parameters, it is important that the discriminator output time constant should be considerably shorter than the reciprocal of the highest modulation frequency which is of importance for the system operation. This will be discussed later in consideration of loop stability and time delay.

PHASE LOCKED LOOP

The basic block diagram of the phase locked loop is now shown in Figure 2.

Assume the input signal applied to the phase detector is an FM carrier of the form

$$v_1(t) = A \cos (\omega_1 t + \phi_1 (t)) \qquad (C8)$$

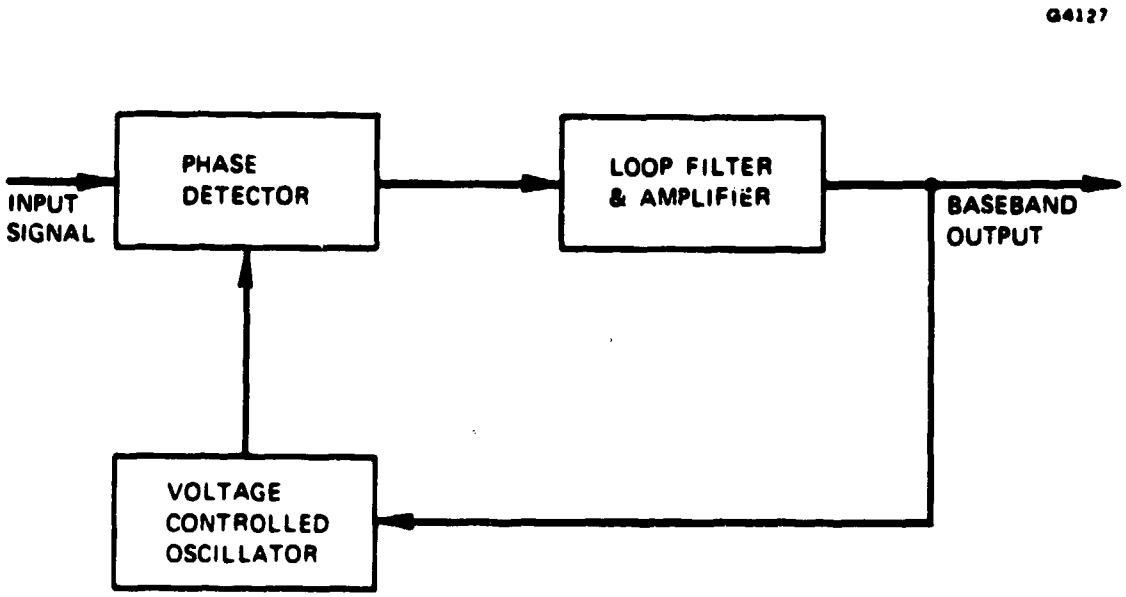


Figure 2 Block diagram of PLL.

where A is the constant amplitude of the carrier, ω_i is the input signal center frequency; and $\phi_i(t)$ is the input signal phase modulation.

Input noise will be neglected for the present. Similarly, the VCO output signal (synchronizing signal) is of the form

$$v_s(t) = -(2/A)\sin(\omega_i t + \phi_r(t)) \qquad (C9)$$

where ω_i is the VCO center frequency, $\phi_r(t)$ is the VCO phase modulation. The particular form of VCO signal is chosen here to indicate a phase locked quadrature relationship between the VCO signal and the input signal. The 2/A amplitude is chosen as a matter of convenience. Both characteristics stem from the multiplier form of phase detector (ideal doubly-balanced mixer).

As mentioned earlier, the static frequency error between the input and VCO signal is assumed to be zero, indicating a locked condition for the loop. The phase detector output signal will be

$$v_i(t) \cdot v_s(t) = -\sin(2\omega_i t + \phi_i(t) + \phi_r(t)) + \sin(\phi_i(t) - \phi_r(t)) \qquad (C10)$$

if the first term in the equation is neglected (upper sideband component) or assumed that it is subsequently rejected by the loop filter, the filter output becomes

$$v_t(t) = G_2 f(t) \circledast \sin\phi_e(t) \qquad (C11)$$

where G_2 is the baseband amplifier gain, f (t) is the impulsive response of the filter,

$$\phi_e(t) = \phi_i(t) - \phi_r(t) \qquad (C12)$$

and Ⓐ denotes convolution. $v_t(t)$ is then the tuning voltage applied to the VCO and baseband output signal. The resultant VCO output signal is a FM signal whose frequency deviation is directly proportional to v_t.

$$d\phi_r(t)/dt = G\, f(t) \circledast \sin \phi_e(t) \qquad (C13)$$

with $G = G_2 G_3$, and G_3 being the VCO sensitivity in radians per volt-seconds.

This equation is a nonlinear differential equation whose general solution is not available; however by restricting $|\phi_e(t)| < \pi/2$ some important loop characteristics may be derived.

Referring back to the input equation C8, we shall now consider the input signal of the form where

$$\phi_i(t) = \Delta\omega_i t + \phi_i'(t) \qquad (C14)$$

$\Delta\omega_i$ represents a static input frequency offset from the center frequency ω_i, and $\phi_i'(t)$ represents a dynamic signal modulation. The loop response will now take the form

$$\phi_r(t) = \Delta\omega_i t + \phi_r'(t) + \phi_o \qquad (C15)$$

where ϕ_o is a constant phase error (a function of loop gain) due to $\Delta\omega_i(t)$. $\phi_r'(t)$ is the dynamic signal modulation response. By substitution of equation C14 and C15 into equation C13 we obtain the result

$$\Delta\omega_i + d\phi_r'(t)/dt = G\, f(t) \circledast \sin(\phi_e'(t) - \phi_o) \qquad (C16)$$

here

$$\phi_e'(t) = \phi_i'(t) - \phi_r'(t)$$

the dynamic phase error.

The iesign of the loop should be such that the phase error $\phi_e'(t) < 1$ rad (determines impulse noise), then the sine function can be approximated bv

$$\sin(\phi_e'(t) - \phi_o) \cong \phi_e'(t) \cos\phi_o - \sin\phi_o \qquad \text{(C17)}$$

Equation C16 may be written in two parts

$$\Delta\omega_i = -G\ f(t) \circledast \sin\phi_o \qquad \text{(C18)}$$

represents the static equation and

$$d\phi_r'(t) = G \cos\phi_o\ f(t) \circledast (\phi_i'(t) - \phi_r'(t)) \qquad \text{(C19)}$$

represents the linearized dynamic tracking equation.

By taking the Laplace transforms of both equations the transfer characteristic equations may be derived as

$$\sin\phi_o / \Delta\omega_i = -1/G\ F(o) \qquad \text{(C20)}$$

and

$$S\phi_r'(s) = G \cos\phi_o\ F(s)\ (\phi_i'(s) - \phi_r'(s)) \qquad \text{(C21)}$$

or

$$\frac{\phi_r}{\phi_i}(s) = \frac{G(\cos\phi_o)\,F(s)}{S + G(\cos\phi_o)\,F(s)} \qquad (C22)$$

where

$$F(s) = \mathcal{L}(f(t)).$$

Equation C22 is based on a small dynamic phase error; however, under noisy signal conditions, the phase error magnitude may increase beyond $\pi/2$ radians, causing loss of synchronism commonly known as cycle skipping or impulse noise. This nonlinear noise performance produces additional loop output noise that tends to degrade the output signal-to-noise ratio below that predicted by the linear model. This degradation marks the onset of threshold in FM demodulators. By careful loop design, the factors that bring forth the threshold may be restricted, such that the phase locked loop serves as a low-threshold demodulator.

First the effect of noise on the loop will be treated in the region above threshold. The loop will respond to the input noise, resulting in a noise component of phase modulation in the VCO output. The phase detector output will then consist of a signal component that contains both signal and noise terms.

The expression for the input signal with noise may be written as

$$v_i(t) = A\cos(\omega_i t + \phi_i(t)) + N(t) \qquad (C23)$$

then the VCO output contains a signal term and a noise term

$$v_s(t) = -(2/A)\sin(\omega_i t + \phi_{rs}(t) + \phi_{rn}(t)) \qquad (C24)$$

the phase detector output signal is of the form

$$ed(t) = \sin(\phi_{es}(t) - \phi_{rn}(t)) + n(t) \qquad (C25)$$

where

$$n(t) = -(2N(t)/A) \sin(\omega_i t + \phi_r(t)) \qquad (C26)$$

and

$$\phi_{es}(t) = \phi_i(t) - \phi_{rs}(t) \qquad (C27)$$

Again the assumption will be made that a small dynamic phase error exists. The input noise may be represented by

$$N(t) = x(t) \cos \omega_i t - y(t) \sin \omega_i t$$

from equation C26.

$$n(t) = -(2/A)(x(t) \cos \omega_i t - y(t) \omega_i t) \sin(\omega_i t + \phi_r(t)) \qquad (C28)$$

then

$$n(t) = -(x(t)/A) \sin \phi_r(t) + (y(t)/A \cos \phi_r(t)) \qquad (C29)$$

the $2\omega_i$ terms were deleted since they would normally be filtered out by the loop.

We now need to know the power spectral density of n(t). This is a complex problem, since $\phi_r(t)$ is in part derived from n(t) and in part determines n(t). For the case where N(t) has a symmetrical bandpass

spectrial density which is much wider than the bandwidth of $\dot{\phi}_r(t)$, the VCO phase modulation (due to the loop bandwidth), then n(t) is essentially the lowpass analog of N(t) appropriately scaled.

The conclusion is that for small dynamic phase error, as a result of both noise and modulation (above threshold), the phase locked loop may be represented by a linear model with an equivalent noise input. The behavior of this loop below threshold will be reserved for later since basic loop stability and the loop filter should first be considered.

In order to obtain a stable closed-loop system, the conditions necessary to obtain stability depend upon the establishment of a suitable open-loop gain and phase response. In the implementation of a system, the loop inadvertently experiences excess time delay. The sources of this delay are the physical electrical length of the signal path and the presence of high-frequency poles. Both factors are a function of circuit design and can be restricted to tolerable limits; however, they preclude the realization of an arbitrarily wideband system. High frequency poles are due partly to the presence of parasitic and stray energy storage elements as will be incountered in the VCO, loops amplifier and as was mentioned earlier in the phase detector. The time delay may be expressed as

$$\tau = \frac{\phi_b}{\omega_b} \qquad \text{(C30)}$$

where ϕ_b is the excess phase shift, in radians, at the baseband frequency ω_b. It can be shown that the inclusion of the loop time delay, τ, modifies the loop transfer function with a term

$$e^{-\tau s} \qquad \text{(C31)}$$

The closed-loop response F(s), and subsequently the closed-loop noise bandwidth B_n, become a function of the delay (or phase shift ϕ_b).

The open loop response can be determined by considering a modulated input signal with a small phase deviation at the VCO center frequency, where $|\phi_i(t)| \ll 1$ radian and $\Delta\omega_i = 0$, $\dot{\phi}_o = 0$. By breaking the loop

$$\left.\frac{\dot{\phi}_r}{\phi_i}(s)\right|_{\text{open loop}} = G_{oL}(s) = \frac{KF(s)}{s} \qquad \text{(C32)}$$

where K is a scale factor determined by a number of gain constants. The open-loop transfer function provides a means of classifying the various PLL implementations. For this particular application only the third order, type three loop is considered. The loop filter is specially designed to have a complex frequency signal transfer function F(S) given by

$$F(S) = K_f \frac{1 + 2\zeta_z \frac{s}{\omega_z} + \frac{s^2}{\omega_z^2}}{1 + 2\zeta_p \frac{s}{\omega_p} + \frac{s}{\omega_p^2}} \qquad \text{(C33)}$$

where K_f is a preselected filter scale factor, ω_z and ω_p are frequencies of conjugate complex zeros and poles, respectively. ζ_z and ζ_p are respective damping ratios of the complex zeros and poles. By substituting equation C33 into equation C32 we obtain

$$G_{oL}(s) = \frac{1 + 2\zeta_z \frac{s}{\omega_z} + \frac{s^2}{\omega_z^2}}{\frac{s}{K}\left(1 + 2\zeta_p \frac{s}{\omega_p} + \frac{s^2}{\omega_p^2}\right)} \qquad \text{(C34)}$$

where K is a loop scale factor.

The closed-loop gain $G_{cL}(s)$ for the phase-locked loop may be computed from

$$G_{cL} = \frac{G_{oL}}{1 + G_{oL}} \qquad \text{(C35)}$$

By substituting equation C34 into equation C35 we obtain the closed-loop transfer function for the third order loop

$$G_{cL}(s) = \frac{1 + 2\zeta_z \frac{s}{\omega_z} + \frac{s^2}{\omega_z^2}}{1 + \frac{s}{\omega_z}\left(2\zeta_z + \frac{\omega_z}{K}\right) + \frac{s^2}{\omega_z^2}\left(\frac{2\zeta_p \omega_z^2}{K\omega_p} + 1\right) + \frac{s^3}{\omega_p^2 K}} \qquad \text{(C36)}$$

Again if the loop time delay is considered, the term $e^{-s\tau}$ must be inserted into the above equation, therefore

$$\frac{1}{K} \text{ becomes } \frac{1}{Ke^{-s\tau}} = \frac{1}{K} e^{s\tau}$$

replacing in the expression for G(S) we now obtain

$$G_{CL}(S) = \frac{1 + 2\zeta_z \frac{s}{\omega_z} + \frac{s^2}{\omega_z^2}}{1 + \frac{s}{\omega_z}(2\zeta_z) + \frac{s}{K} e^{s\tau} + \frac{S^2}{\omega_z^2} + \frac{S^2}{K\omega_p} 2\zeta_p e^{s\tau} + \frac{S^3}{\omega_p^2 K} e^{s\tau}} \qquad (C38)$$

By careful analysis of equation C34,C38 it can be shown that compensation for the loop time delay can be achieved by the introduction of a zero-pole pair at frequencies above the 0-dB open-loop gain point in the open-loop response characteristic. The net result of this compensation is that of offsetting the increase in noise bandwidth caused by the time delay which in turn results in improved noise performance in the nonlinear noise region (threshold).

Earlier analysis in reference to noise was based on a small dynamic phase error but the discussion on loss-of-lock and cycle-shipping indicated sources for nonlinear noise performance. As was indicated earlier, the nonlinear noise performance produces additional loop output noise degrading the output SNR below that predicted by the linear model. Referring back to the equation of the phase detector output signal

$$e_d(t) = \sin(\phi_{es}(t) - \phi_{rn}(t)) + n(t)$$

and with respect to the loop output

$$\dot{\phi}_r(t) = KF(P)\,[\sin(\phi_{es}(t) - \phi_{rn}(t)) + n(t)] \qquad (C39)$$

where P represents the carrier-to-noise ratio.

The differential equation with respect to the phase error components $\phi_{es}(t)$ and $\phi_{rn}(t)$ will be

$$\dot{\phi}_r(t) = \dot{\phi}_i(t) - \dot{\phi}_e(t) = \dot{\phi}(t) - \dot{\phi}_{es}(t) + \dot{\phi}_{rn}(t) \tag{C40}$$

then

$$\dot{\phi}_{es}(t) - \dot{\phi}_{rn}(t) = -KF(P) \sin (\phi_{es}(t) - \phi_{rn}(t)) - KF(P)n(t) + \dot{\phi}_i(t) \tag{C41}$$

If the term $\phi_{rn}(t)$ is no longer small, the first order effect is that the sine term no longer renders the signal and noise components as additive terms in the loop response. By trigonometric expansion the sine term may be written as

$$\sin (\phi_{es}(t) - \phi_{rn}(t)) = \phi_{es}(t) \cos \phi_{rn}(t) - \sin \phi_{rn}(t) \tag{C42}$$

if $\phi_{es}(t) << 1$.

By expanding cos $\phi_{rn}(t)$ and sin $\phi_{rn}(t)$ in a power series we can obtain

$$-(\dot{\phi}_{es}(t) - \dot{\phi}_{rn}(t)) = KF(P)\left(\phi_{es}(t)\left(1 - \frac{\phi_{rn}^2(t)}{2!} + \frac{\phi_{rn}^4(t)}{4!} - \ldots\right)\right.$$

$$\left. -(\phi_{rn}(t) - \frac{\phi_{rn}^3(t)}{3!} + \frac{\phi_{rn}^5(t)}{5!} - \ldots)\right) + KF(P)n(t) - \dot{\phi}_i(t) \tag{C43}$$

This equation shows some higher-order noise terms ignored in the linear model.

As mentioned before, noise has the effect of creating phase error in the loop. When this error gets large enough, the loop can lose lock and skip one or more cycles. This produces an impulse in the output of the phase locked loop. Of interest is the rate at which the loop loses lock and generates impulses. Unfortunately, this problem has not been solved exactly for an arbitrary loop in the presence of signal modulation. However, Viterbi[1] has solved the problem for a first order loop with no signal modulation. The result of that analysis gives an equation for the mean time to loss of lock.

$$T = \frac{1}{\gamma} \int_0^{2\pi} d\phi \int_{\phi}^{2\pi} dx \exp\left[\alpha(\cos\phi - \cos\chi)\right] \tag{C44}$$

where

$$\gamma = 4B_n/\alpha, \tag{C45}$$

$$B_n = \int_0^{\infty} \left|\frac{G}{1+G}\right|^2 df \tag{C46}$$

and α is the carrier-to-noise ratio in a bandwidth of 2Bn. The quantity, Bn, is the equivalent baseband noise bandwidth of the loop. The rate at which impulses occur is simply

$$N_{IMP} = 1/T \text{ (impulses/sec)} \tag{C47}$$

In general, an indication of loop behavior with respect to impulse noise can be obtained by evaluating equation C44 with the lower limit of integration (zero) being replaced by ϕ_e, where ϕ_e as stated earlier is the phase error due to signal modulation. However, such an extension of equation C44 is not mathematically rigorous.

Loop Bandwidth Requirements for Color Television Signals

Our attention will now be directed toward the application of the phase locked loop in the demodulation of a frequency modulated color television signal. In this circumstance it is not the minimum phase error that is used as a criterion for determining the required phase locked loop bandwidth. Instead, the smallest loop bandwidth for which the three sigma phase error does not exceed $\pi/2$ is the criterion. More precisely,

$$3\sigma_T = \pi/2 \tag{D1}$$

where σ_T is the standard deviation of the total phase error. The total phase error, σ_T^2, has two components: the phase error due to thermal noise, σ_{th}^2, and the phase error due to the modulation error, σ_m^2. The error due to thermal noise is given by

$$\sigma_{th}^2 = \frac{N_0}{C} B_n \tag{D2}$$

where B_n is the loop bandwidth and C/N_0 is the carrier-to-one-sided noise spectral density ratio. The modulation error is

$$\sigma_m^2 = \frac{\Delta P^2}{2\pi} \int_{-\infty}^{\infty} |1 - G(j\omega)|^2 S_\phi(\omega) d\omega \tag{D3}$$

where ΔP is the rms radian frequency deviation, $S_\phi(\omega)$ is the phase spectrum of the input signal m(t) and $G(j\omega)$ is the closed loop transfer function. The phase spectrum of color TV will be discussed later. The equations D2 and D3 were evaluated for various color spectra and values of Bn. The total phase error, σ_T^2, is

$$\sigma_T^2 = \sigma_{th}^2 + \sigma_m^2 \qquad \text{(D4)}$$

Combining D1 and D4 gives

$$\sigma_m^2 = \frac{\pi^2}{36} - \sigma_{th}^2 \qquad \text{(D5)}$$

For a given Bn, σ_{th}^2 is readily calculated from D2, which gives σ_m^2 from D5. Next ΔP is calculated from equation D3. In this way Bn may be plotted as a function of ΔP for a given color TV spectrum. The frequency distribution in a color television is shown in Figure 3. The black and white portion of this frequency spectrum was modeled by an envelope function of the form

$$S_u(f) = A\,(f-fo)^{\lambda}\, e^{-\alpha(f-f_o)} \qquad \text{(D6)}$$

It follows directly, that in decibels, the black and white part of the power spectrum is of the form

$$S(f)_{dB} = B + \mu \log (f-fo) + B\,(f-fo) \qquad \text{(D7)}$$

This function is one of the Pearson curves (see "Mathematical Methods of Statistics," by H.G. Cramer). The normalized envelope function for the black and white part of the color TV power spectrum is

$$S(f)_{B+W} = -37.9088 - 10.6952 \ln (f+0.0254) - 2.7804\,(f+0.0254)$$

where f is in MHz and $S(f)_{B+W}$ is in dBw per 15.75 kHz. If we let $S_v(f)$ be defined as

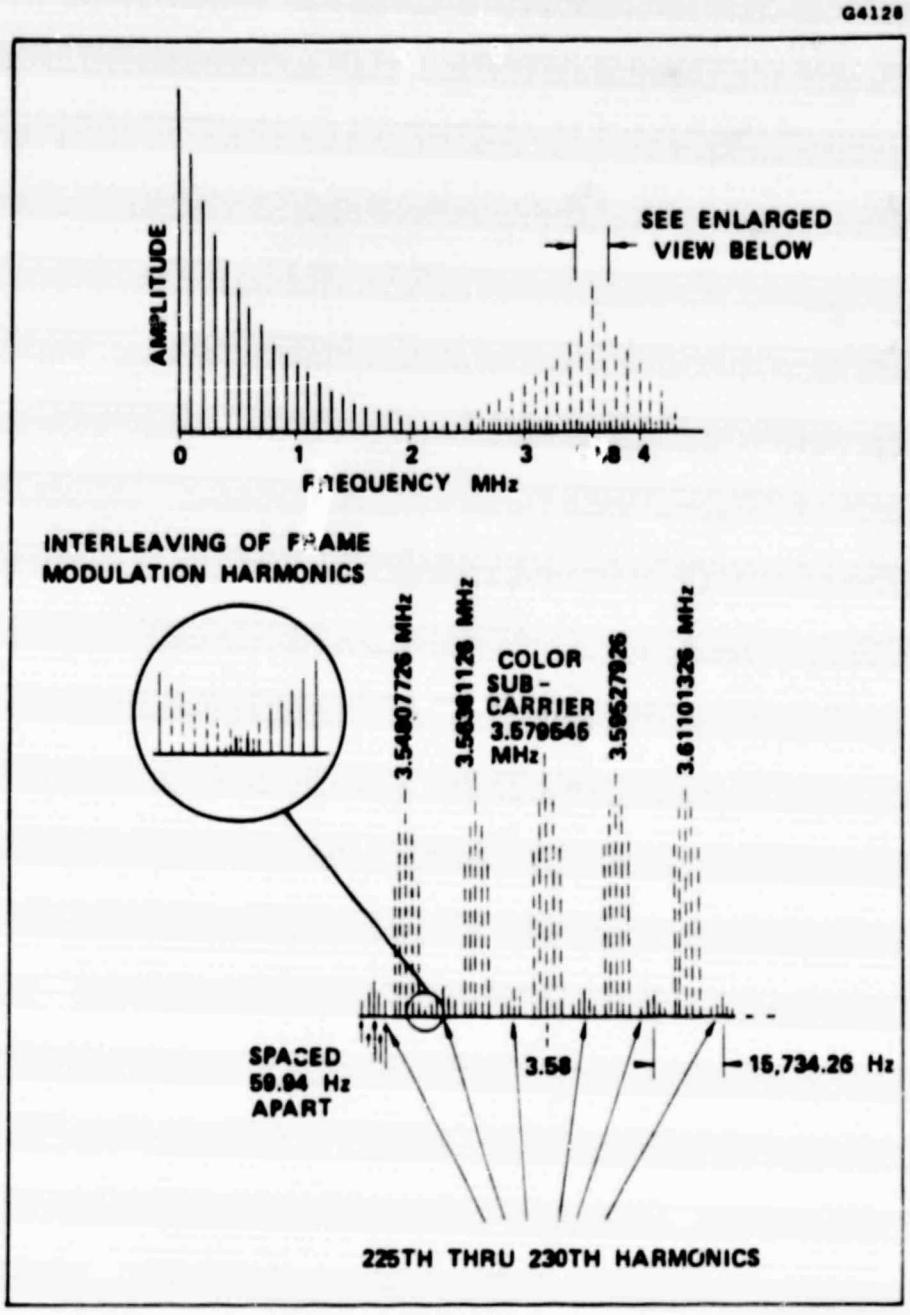


Figure 3. Frequency Distribution in a Color Television Signal

$$S_v(f) \begin{cases} = \\ \\ \\ \\ \end{cases} \begin{array}{l} 0 \text{ for } f < 2.25 \\ 16f^2 - 75.14f + 83.28 \text{ for } 2.25 \leq f < 3.58 \\ -464076 + f(580027 + f(-289291 + f(71980 \\ + f(-8935.35 + 442.737f)))) \text{ for } 3.58 \leq f < 4.45 \end{array} \qquad \text{(D8)}$$

then the color part of the power spectrum $S(f)_c$, in the same units, is given by

$$S(f) = 2S_v(f) - 60 \text{ dBw per } 15.75 \text{ kHz}$$

The phase spectrum is related to the frequency spectrum by

$$S_\phi(\omega) = \frac{S(\omega)}{\omega^2} \qquad \text{(D9)}$$

The emphasis function

$$E(f) = 2.2387 \left[\frac{\frac{1}{4.67} + \left(\frac{f}{0.404}\right)^2}{4.67 + \left(\frac{f}{0.404}\right)^2} \right] \qquad \text{(D10)}$$

is inserted into equation D3 which then becomes

$$\sigma_m^2 = \frac{1}{P} \frac{\Delta P^2}{(2\pi)^2} \int_o^{fc} \frac{S(f)\ E(f)\ |\ 1-G(jw)\ |^2}{f^2} df \qquad \text{(D11)}$$

where fc = 4.2 MHz is the upper cutoff frequency and P is the normalization factor given by

$$P = \int_{0}^{fc} S(f)\, E(f)\, df \qquad \text{(D12)}$$

Video Signal to Noise Ratio

Earlier the analysis of the phase locked loop was treated under conditions of noise both above and below threshold. We shall now show the relationship between an input carrier to noise ratio defined in a given predetection bandwidth to the output video signal to noise ratio. Noise has the effect of modifying the carrier signal as shown in Figure 4.

Here the noise vector $\overline{n}$ has components x and y parallel and orthogonal respectively to the signal carrier vector, $\overline{A}$. Both phase and amplitude noise are created, but only phase noise is of importance here provided that the noise is above threshold. This phase noise as observed from Figure 5 is given by the equation

$$\phi n(t) = \tan^{-1} \frac{y(t)}{A+x(t)} \qquad \text{(E1)}$$

For reasonably large carrier to noise ratios, this can be approximated as

$$\phi n(t) = y(t)/A \qquad \text{(E2)}$$

since x and y are small compared to A.

This phase noise produces a noise voltage V_{tn}, at the input of the voltage controlled oscillator. The noise voltage V_{tn} is important in determining the signal to noise ratio (S/N).

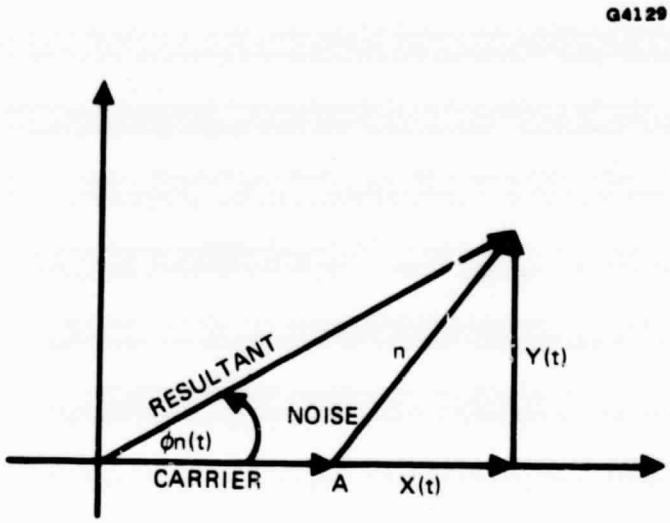


Figure 4. Phasor Representation of Carrier and Noise Without Modulation

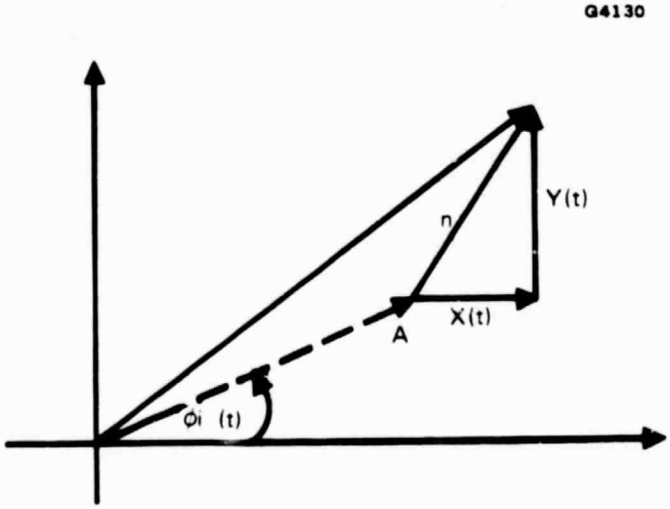


Figure 5. Phasor Representation of Carrier and Noise With Modulation

Using the previously derived loop equations, it can be shown that the mean squared noise voltage at the output of the loop is

$$\overline{V_{tn}^2} = \frac{8\eta_o}{K^2A^2} \int_o^\infty \left| \frac{\omega G}{1+G} \right|^2 df, \qquad \text{(E3)}$$

where $\eta_o = \overline{y^2}$ is the input noise power spectral density. If the signal is subsequently processed through a rectangular video filter with cutoff at frequency f_b, the noise voltage is

$$\overline{V_n^2} = \frac{8\eta_o}{K^2A^2} \int_o^{f_b} \left| \frac{\omega G}{1+G} \right|^2 df \qquad \text{(E4)}$$

since in most systems $G/(1+G) \cong 1$ in baseband, equation E4 reduces to

$$\overline{Vn^2} = \frac{8\eta_o\ \omega_b^2\ fb}{3K^2A^3} \qquad \text{(E5)}$$

A frequency modulated test tone signal of deviation ω_d will produce a signal

$$\overline{V_s^2} = 2\omega_d^2/K^2 \qquad \text{(E6)}$$

now if equation E6 is divided by E5, we obtain the signal-to-noise ratio (SNR).

$$SNR = 3\frac{\omega_d^2}{\omega_b^2} \cdot \frac{A^2}{4\eta_o\ f_b} \qquad \text{(E7)}$$

Realizing that ω_d/ω_b is the modulation index m, that $A^2/2$ is the carrier power C and that $2\ m_o f_b$ is the noise power in twice the baseband frequency bandwidth, we obtain the standard FM improvement formula

$$S/N = 3m^2\ (C/N)_{AM} \tag{E8}$$

where $(C/N)_{AM}$ is the carrier to noise ratio for an AM system. In FM communications it is common to express SNR in terms of the carrier to noise ratio in the IF bandwidth, B_{IF} in which case

$$S/N = 3m^2\ (B_{IF}/2fm)(C/N) \tag{E9}$$

where fm is the highest baseband modulating frequency.

For a television signal, the S/N ratio is defined as the peak-to-peak luminance signal (no sync pulse) divided by the weighted noise. In television signal measurements all measurements are referenced to a peak-to-peak video signal of one volt. The luminance component of the video signal is 0.714 volts, the remainder being the sync pulse. The luminance signal expressed in dB below the composit signal is therefore

$$20 \log (1/0.714) = 2.9 \text{ dB} \tag{E10}$$

Since the rms weighted noise is being compared to a peak to peak signal level, another correction factor is utilized. It takes the form

$$20 \log \frac{\text{Sine wave peak-to-peak}}{\text{Sine wave } V_{ms}} = 20 \log 2\sqrt{2} = 9 \text{ dB} \tag{E11}$$

The combined effect of the de-emphasis circuit and the noise weighting filter will provide a noise improvement factor of 13 dB.

The addition of these correction factors, equation E9 will now become the FM improvement formula for television expressed in dB

$$S/N|_{video} = 10 \log \left[3m^2 (B_{IF}/2_{fm}) \right] + (C/N)dB + 9dB - 2.9dB + 13dB \quad \text{(E12)}$$

Assuming that the deviation ratio, m = 2.86, and the video baseband upper frequency to be 4.2 MHz, equation E12 now becomes

$$S/N|_{video} = 39.3dB + (C/N)dB. \quad \text{(E13)}$$

APPENDIX B

ACCEPTANCE TEST PLAN FOR 12 GHz SATELLITE VIDEO RECEIVER NASA-GODDARD SPACE TEST CENTER CONTRACT NO. NAS 5-24421

W-42953

ACCEPTANCE TEST PLAN FOR
12 GHz SATELLITE VIDEO RECEIVER
NASA-GODDARD SPACE TEST CENTER
CONTRACT NO. NAS 5-24421

OCTOBER 1978

HUGHES AIRCRAFT COMPANY
ELECTRON DYNAMICS DIVISION
3100 WEST LOMITA BOULEVARD
TORRANCE, CALIFORNIA 90509

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1.0 GENERAL INFORMATION

The tests described in the following procedure are to verify the proper system performance of the 12 GHz satellite video receiver. If system specifications are not met, the test set up should be verified for proper operation.

Use of the required test equipment listed in the next section should follow proper operation procedures as specified by the equipment manufacturers instruction manuals. When equipment is substituted for the suggested test equipment, adequate consideration should be given as to what effect, if any, will be had on the system performance.

The tests can be conducted at any of the transponder frequencies in the 11.7 to 12.2 GHz range, that is up from 11.73 GHz at 40 MHz increments. However, for the purpose of evaluating the prototype receiver, these tests are performed with the transponder frequency at 12080.5 MHz. The test procedure is divided into two main sections. First, the Downconverter Unit is tested to measure its electrical performance. Then, the Downconverter and Demodulator Units are tested together to prove conformance with the RF, video, and audio specifications.

The tests are for an RF signal, either CW or modulated by a full-field video test signal, received from a test transmitter. Most video tests apply equally well to on-line vertical interval test signals (VITS), provided there is insignificant signal degradation due to the satellite uplink transponder. The performance objectives apply irrespective of the average picture level (APL) within the APL range 10 percent to 90 percent. This is an important point to remember when making VITS measurements, particularly during program transmission periods where control cannot be exercised over the APL value of picture signal. Many of the transmission parameters can be markedly affected by APL variations. Accordingly, the operator should allow sufficient time when making VITS

measurements to ensure a good portion of the APL range is explored by the picture signal before recording the test signal measurement. In every case the highest distortion measurement observed during this period should be recorded and then compared with the performance objective to determine whether or not the facility is within the stated objective.

Video waveform measurement techniques used in these tests are based on the IRE scale units of measurement (see Figure 1-1a) except where specifically noted otherwise. The waveform technology used throughout the procedure is in accordance with the definitions shown in Figure 1-1b wherein the standard composite color video signal is defined.

The two principal test signals that are required to conduct the various video measurements described in this procedure are:

A. The composite test signal shown in Figure 1-1c, which consists of a line bar, a 2T pulse, a chrominance pulse, and a 5-riser staircase signal.

B. The combination test signal shown in Figure 1-1d, which consists of a white flag, a multiburst and a 3-level chrominance signal.

When conducting in-service VITS measurements the composite test signal shall be inserted on line 17, field 1, and the combination test signal shall be inserted on line 17, field 2.

The modulated RF test signal contains a frequency modulated video signal with a baseband bandwidth of 4.2 MHz and peak deviation of 10.0 MHz, and a frequency modulated audio signal with a subcarrier frequency of 5.14 MHz, peak deviation (C by SC) of 630 KHz, subcarrier bandwidth of 160 KHz, audio bandwidth of 15 KHz, and peak deviation of 60.0 KHz.

This test procedure has been organized to minimize the required test set-up time.

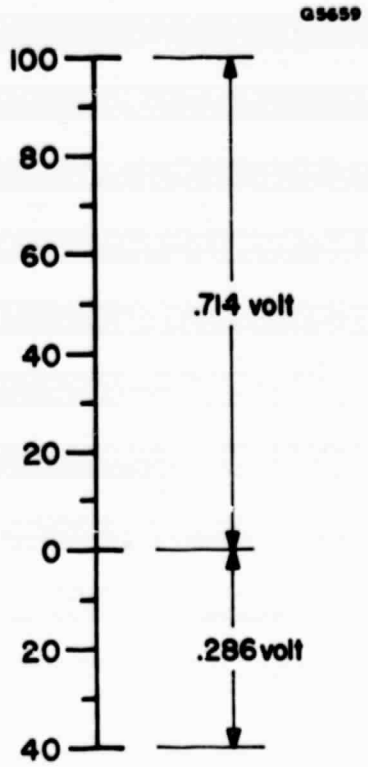
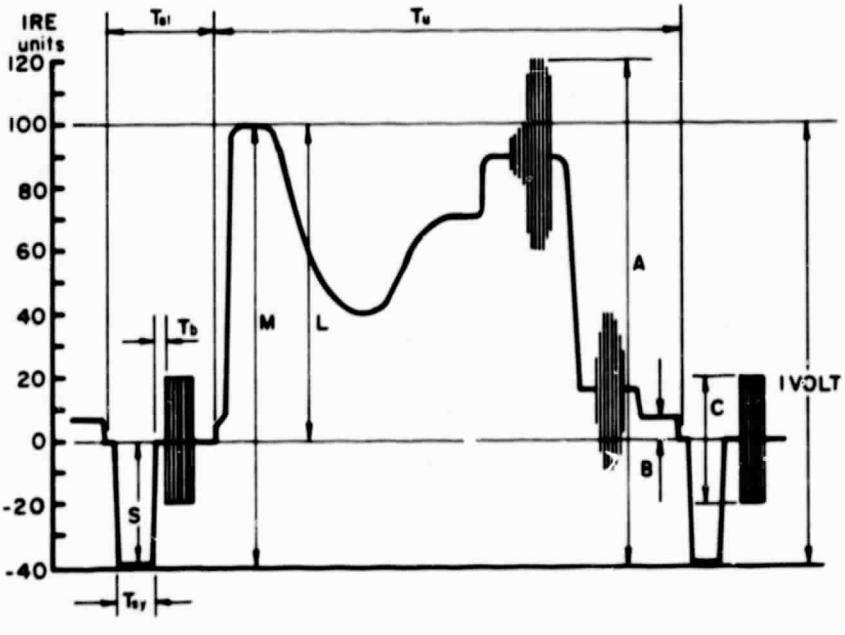


Figure 1-1a The IRE scale units.
(For a 1V P-P composite signal.)



WAVEFORM TERMINOLOGY

A: The peak-to-peak amplitude of the composite color video signa
B: The difference between black level and blanking level (set-up)
C: The peak-to-peak amplitude of the color burst
L: Luminance signal - nominal value
M: Monochrome video signal peak-to-peak amplitude (M=L+S)
S: Synchronizing signal - amplitude
T_b: Duration of breezeway
T_{sl}: Duration of line blanking period
T_{sy}: Duration of line synchronizing pulse
T_u: Duration of active line period

Figure 1-1b The standard composite color video signal.

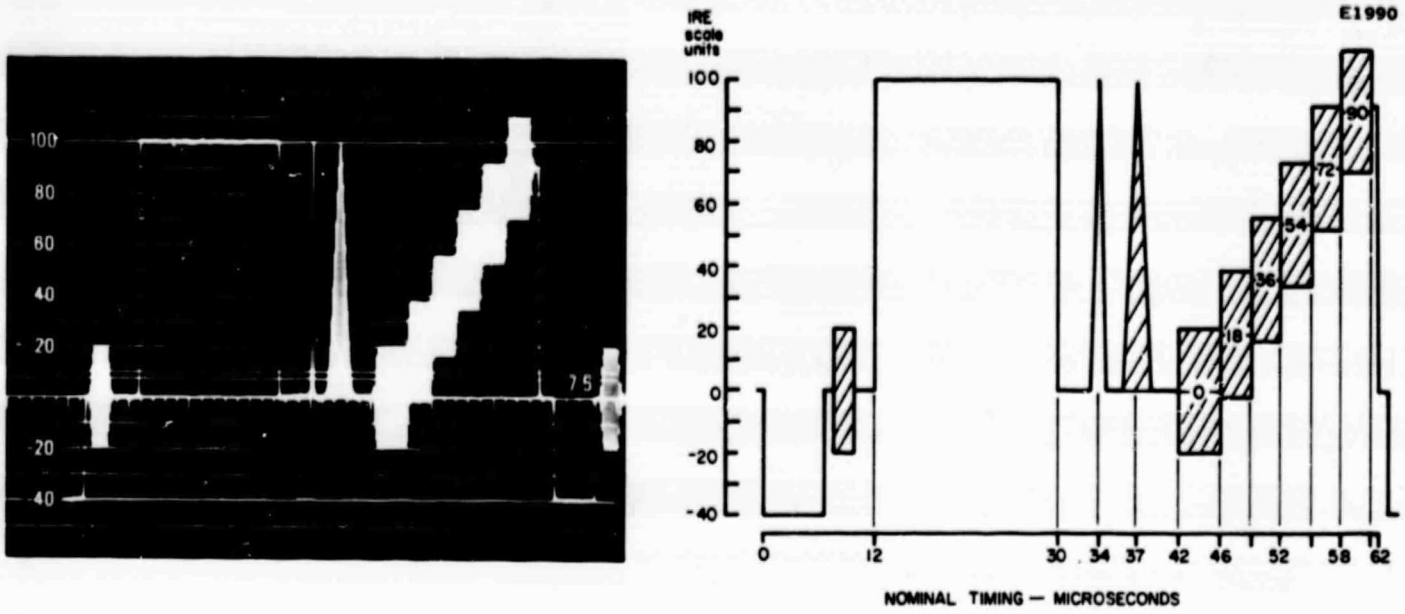


Figure 1-1c The composite test signal.

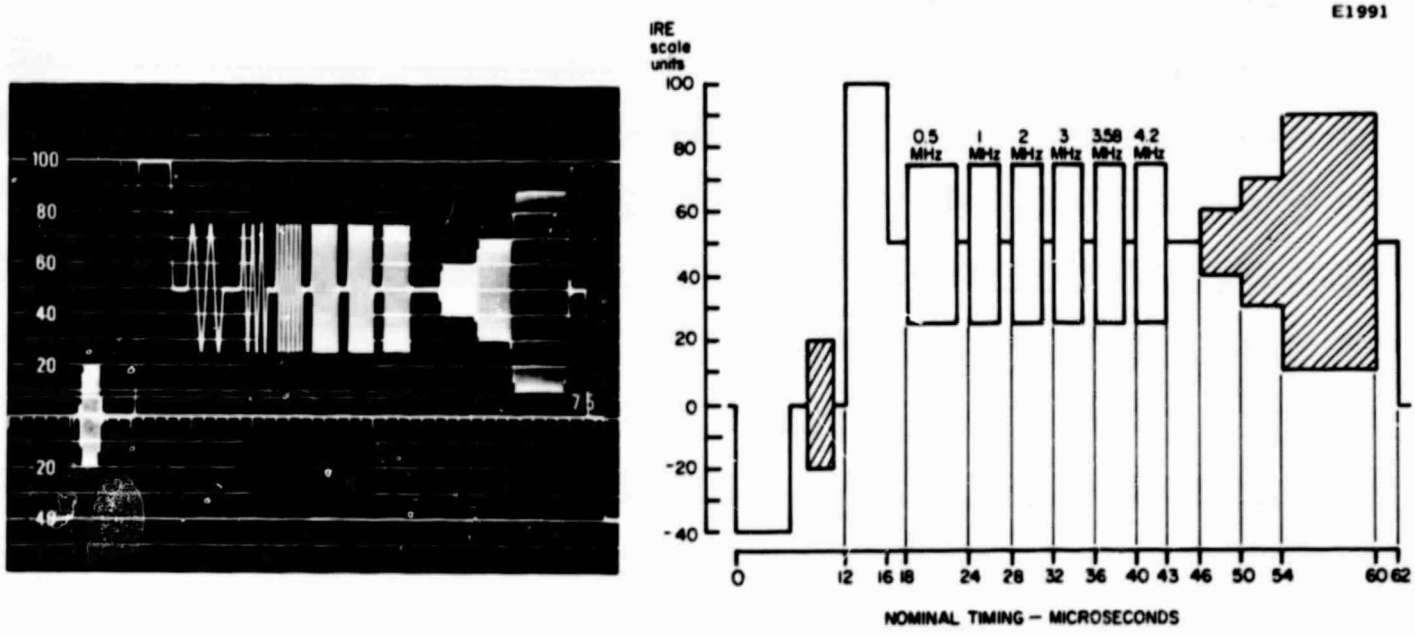


Figure 1-1d The combination test signal.

2.0 TEST EQUIPMENT REQUIRED

The following test equipment, or equivalent, is required.

Model	Description	Manufacturer
	Test transmitter	Hughes
	Assorted attenuator pads	HP
5000A	Signal generator	Systron-Donner
	WR75 10 dB coupler	HP
	WR75 matched load	HP
792	WR75 Variable Attenuator	Narda
8481A	Power Sensor	HP
435A	Power Meter	HP
400E	RMS Voltmeter	HP
7616	Solid State Noise Source	AILTECH
75	Noise Figure Meter	AILTECH
5342A	Frequency Counter	HP
141T	Spectrum Analyzer System	HP
	30 MHz Amplifier 20 dB gain	Hughes
SRA11	1 GHz Mixer	Minicircuits
147A	NTSC Video Signal Generator	Tektronix
	1.0 KHz Low Pass Filter	Hughes
	50 Ω load	HP
011-0102-00	75 Ω load	Tektronix
011-0103-02	75 Ω Termination	Tektronix
7603	Oscilloscope	Tektronix
520A	NTSC Vector Scope	Tektronix
1480	Video Waveform Monitor	Tektronix
8640B	Audio Signal Generator	HP
	Audio Pre-emphasis network	Hughes
8640B	Audio Subcarrier Generator	HP
334A	Distortion Analyzer	HP

Model	Description	Manufacturer
	EIA Noise Test 10 KHz High Pass	Hughes
015-0214-00	Weighting Network	Tektronix
015-0212-00	4.2 MHz Low Pass	Tektronix
146	NTSC Generator	Tektronix
670	Matrix Monitor	Tektronix
1478	Cal Chrominance Level Corrector	Tektronix
	1 GHz, 20 dB Gain Amplifier	Hughes
2001	1 GHz Signal Generator	Wavetek

3.0 DOWNCONVERTER TEST PROCEDURE

This test confirms the electrical performance of the Downconverter and the dynamic range of the receiver.

The test equipment is set up as shown in Figure 3-1. The RF level of the test transmitter signal, tuned to one of the transponder frequencies and without modulation, is attenuated to reduce the power level present at the RF waveguide input of the Downconverter (J1) to between -72 and -87 dBm.

Connect the DC power cable between the downconverter (outdoor unit) and the demodulator (indoor unit). Apply the 115 VAC power to the indoor unit.

3.1 DOWNCONVERTER GAIN

Set the RF input at J1 to 12.08 GHz and at a level of -72 dBm. Connect the power meter to connector J2 using the type F to type N connector adapter. The downconverter IF output level at J2 should be -20 dBm ±6 dB. The gain at this level is plus 52 dB. Record this gain on the data sheet.

3.2 LOCAL OSCILLATOR STABILITY

With the RF input to the Downconverter from the test transmitter tuned to 11.750 GHz ±0.1 MHz, measure the output frequency, F_{IF}, from the IF port. The local oscillator frequency is 11.750 GHz minus F_{IF}, and should be 10.750 GHz ±40 MHz over temperature from -35°C to +50°C. Record this calculated LO frequency on the data sheet.

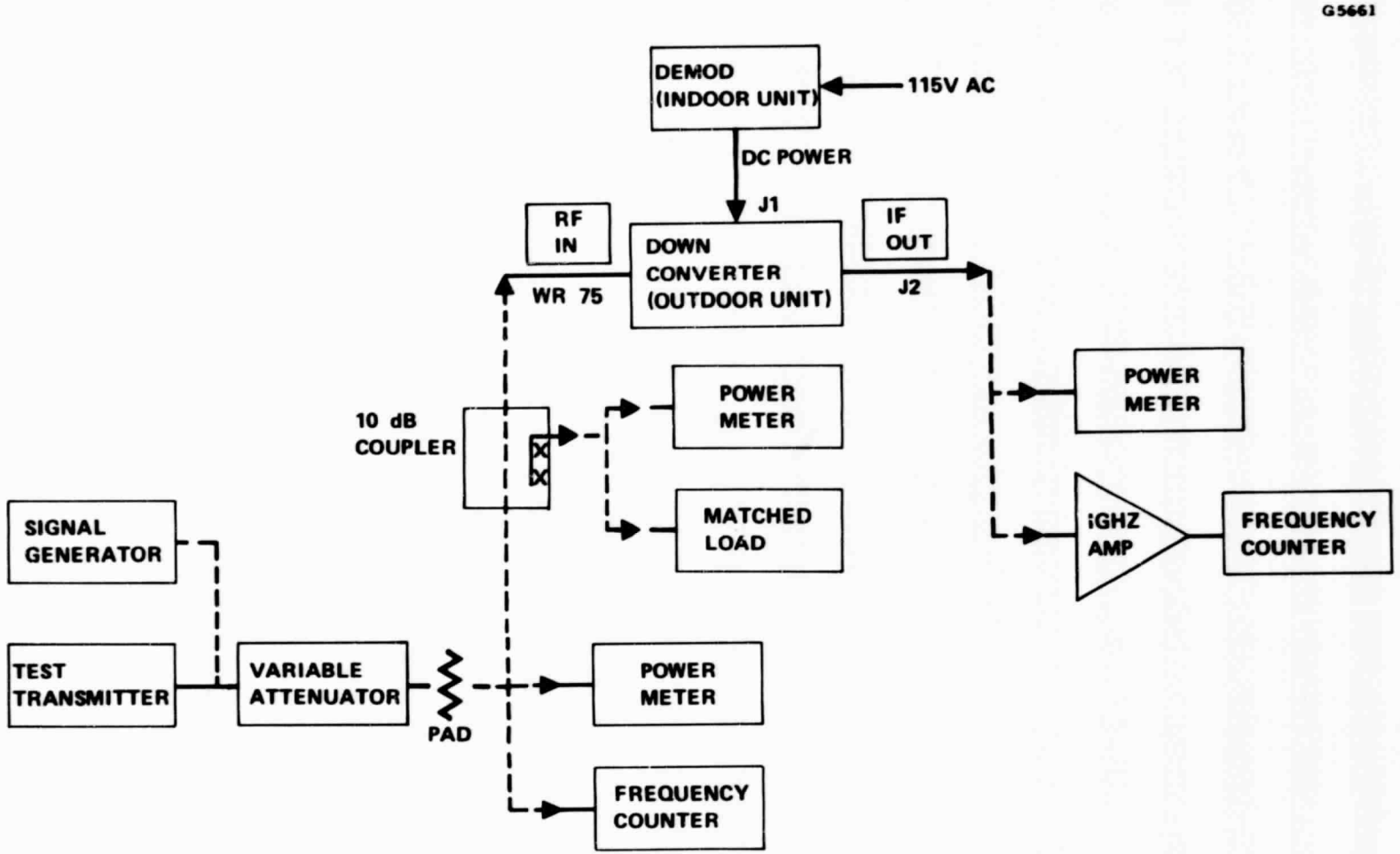


Figure 3-1 Downconverter Test.

3.3 RF INPUT VSWR

With the test transmitter at 12.08 GHz and 0 dBm, measure the return loss from the Downconverter input port J1 by measuring the power level at the coupled arm of the 10 dB coupler (after referencing the coupled level for a shorting plane in place of the Downconverter). This return loss, L_R, should be greater than 10 dB. Record the VSWR on the data sheet. The VSWR is calculated by

$$\text{VSWR} = \frac{1 + \rho}{1 - \rho}$$

where $\rho = 10^{(L_R/20)}$, L_R is the power reflection coefficient measured in dB.

3.4 IMAGE REJECTION

Tune a signal generator from 9.3 to 9.8 GHz with the power level set at -72 dBm. With this signal at J1 measure the IF power level at J2. The power level should be greater than 15 dB below the passband level. Record this image rejection on the data sheet.

3.5 RECEIVER NOISE FIGURE

The receiver noise figure is determined by measuring the noise figure for the Downconverter Unit and adding 0.01 dB to account for the worst case noise figure of 25 dB for the 100 foot long IF cable plus Demodulator Unit. The Downconverter noise figure is most easily determined by using a calibrated automatic noise figure set-up as shown in Figure 3-2.

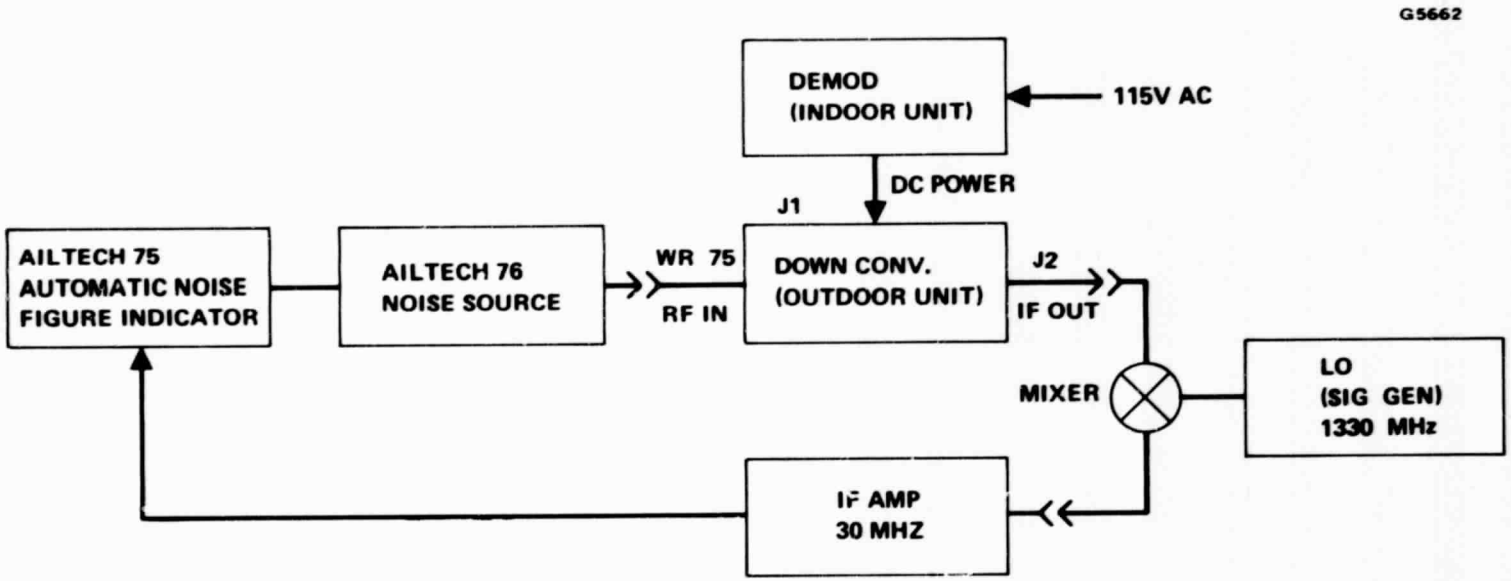


Figure 3-2 Noise figure measurement.

4.0 DEMODULATOR TEST PROCEDURE

These tests prove the conformance of the receiver to the RF, video, and audio specifications.

4.1 RF PARAMETERS

The test equipment is set up as shown in Figure 4-1. The signal input to the Downconverter Unit (at J1) is an RF signal, at a -72 to -87 dBm power level, from the test transmitter. The RF signal is modulated at a peak deviation of 10.0 MHz by the composite video test signal from the video generator with a baseband bandwidth of 4.2 MHz and is tuned to 12.08 GHz.

The correct pre-emphasis is provided by the video transmitter as defined by CCIR Rec. 405-1 for 525 line video. This will be called the standard RF input signal. The output of the Downconverter unit, J2, is connected to the input of the Demodulator Unit, J1.

4.1.1 Channel Filter Test

Since the channel filter (IF filter) is an integral part of the unit, it cannot be tested without disassembly of the demodulator unit, however, an incorrect filter bandwidth would become evident when performing the static and dynamic threshold tests. Accuracy of the filters center frequency would also become evident when performing the differential phase measurement. Based on this rational, no attempt will be made to make a direct measurement of the filter bandwidth or center frequency during this acceptance test.

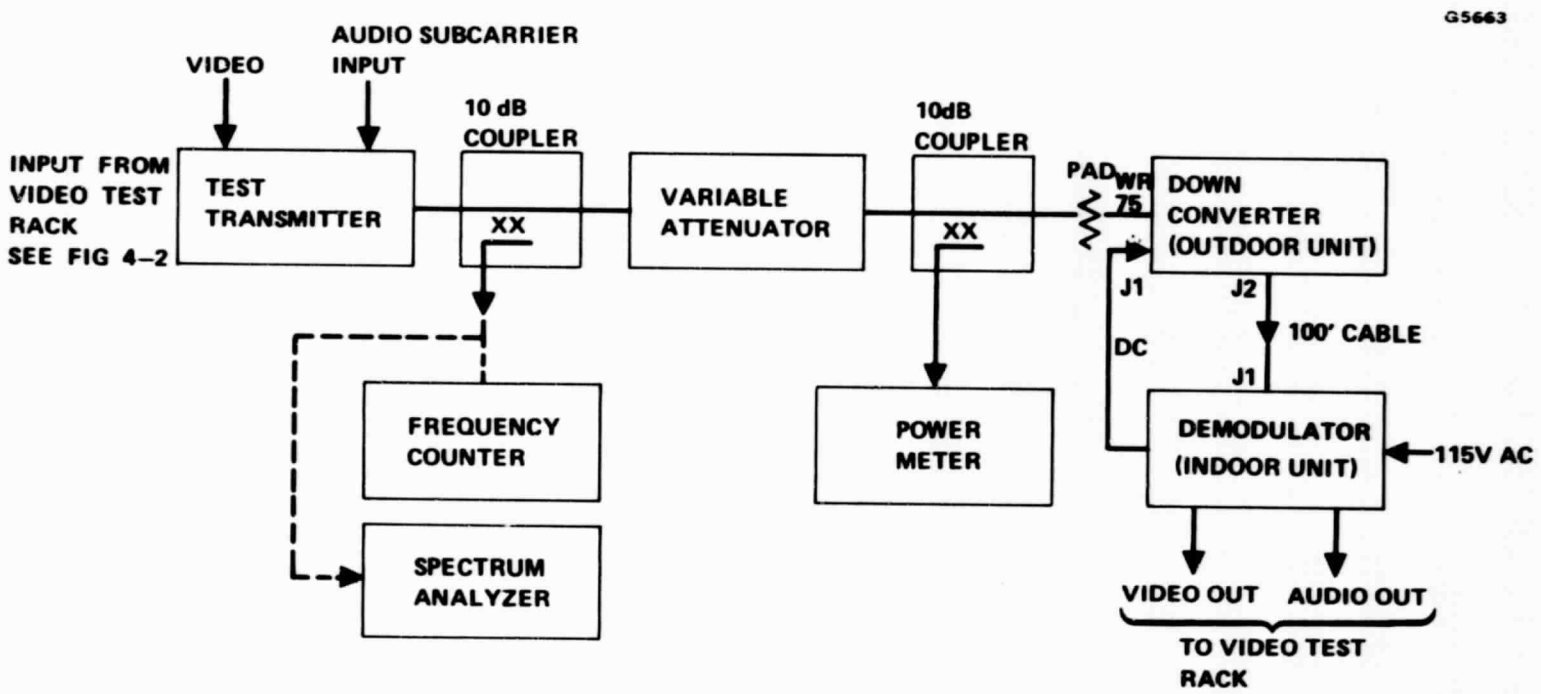


Figure 4-1 Receiver Test.

4.1.2 Dynamic Range, Static Threshold and Signal-to-Noise

Connect the equipment as shown in Figure 4-1. For the static threshold test, the input signal to the unit will be unmodulated, however, the video output level of 1 volt peak-to-peak must first be established using the proper video modulated signal at the input to the receiver. The correct video deviation of the test signal is established using the carrier null method, and referenced to 760 KHz, the 0 dB crossover point on the video pre-emphasis curve as given in the CCIR Recommendation 405-1.

After the video deviation has been properly set, the transmitter RF output level is set to -72 dBm and this signal connected to the input of the receiver outdoor unit.

The demodulated video signal at the output of the receiver is now observed on a waveform monitor which has been properly terminated into 75 ohms. See Figure 4-2. The receiver video output control should now be adjusted to exactly 140 IRE units as observed on the waveform monitor display. This establishes the receiver output level at 1 V p-p.

Remove the video modulation from the transmitter and connect the receiver output to the RMS voltmeter through the proper network and termination as shown in Figure 4-2. For the following measurements the clamping circuit on the signal processor board is disengaged by jumpering test points TP6 and TP7 on the board. This is done to assure that no clamping pulses occur which would reduce the noise content at the video output port and thus give an erroneous signal-to-noise ratio. This measurement will result in a worst case performance and under normal conditions with video present and with the clamping circuit engaged, the video performance will be at least as good as this measurement. Measure the noise level as indicated on the RMS voltmeter and record

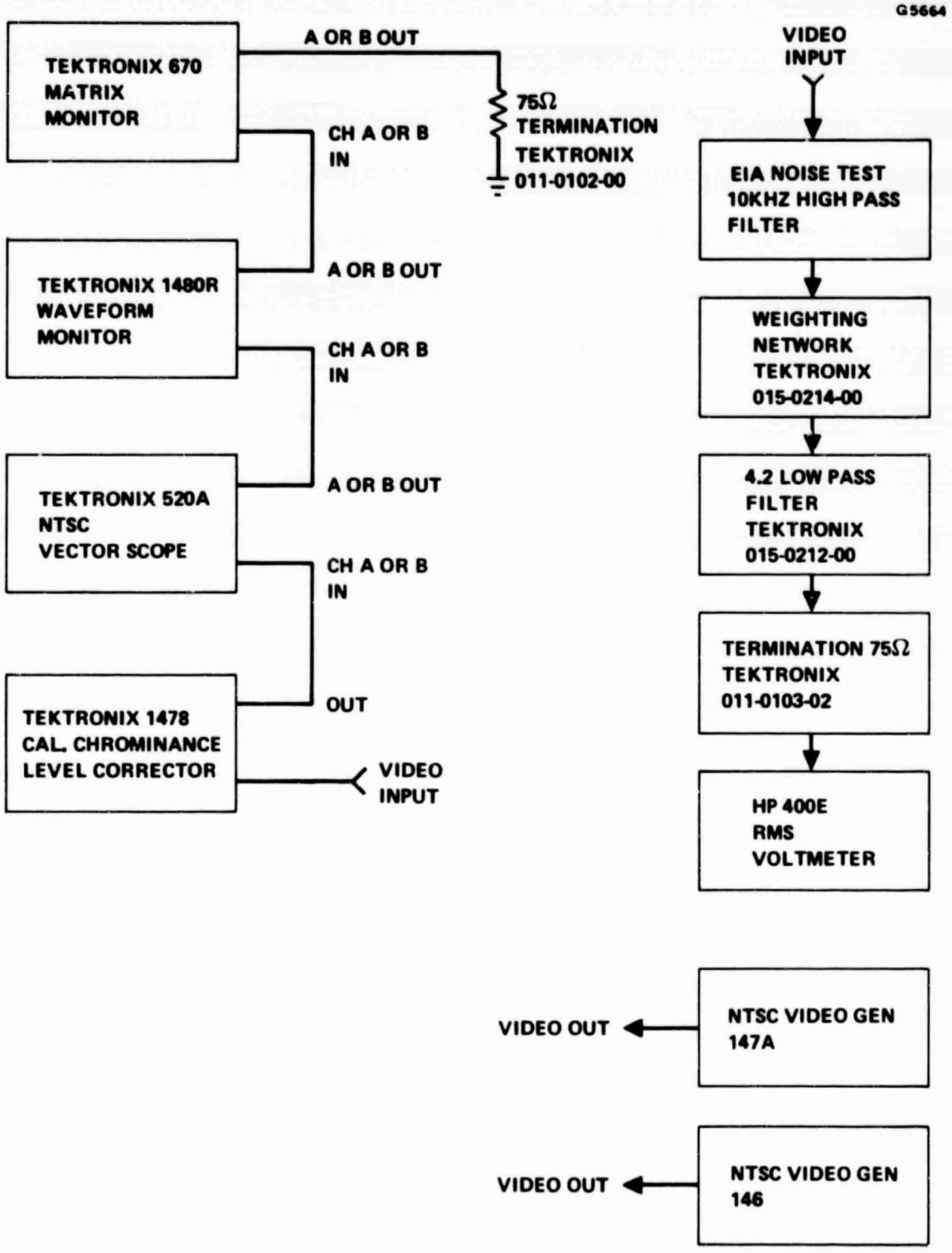


Figure 4-2 Video test rack.

this value. The RF signal at the input to the receiver is now adjusted downward in exactly 1 dB steps and the RMS voltmeter readings are recorded for each step. This procedure is continued until a receiver input level of -87 dBm is obtained. The receiver output signal-to-noise ratio vs. input level in dB is now computed using the formula:

$$S/N_S \text{ dB} = 20 \log \left(\frac{0.714 \text{ V.}}{\text{RMS meter reading}} \right)$$

The Static Threshold and Dynamic AGC range can be obtained from this data, however, the receiver carrier-to-noise ratio as related to the input signal must be computed.

$$C/N_i \text{dB} = RF_{in} - (KT + IF_{np} + NF)$$

Where:

C/N_idB = The predetection carrier-to-noise ratio in dB

RF_{in} = Receiver input power in dBm

KT = -174 dBm

IF_{np} = 10 log (IF noise bandwidth in Hz) = 10 log (30×10^6 Hz)
= 74.77 dB

NF = Receiver input noise figure in dB

The signal-to-noise ratio vs. carrier-to-noise ratio may now be plotted and compared against the FM Improvement curve to obtain the static threshold characteristic. The FM Improvement curve may be obtained from from the formula:

$$S/N_v \text{dB} = 10 \log \left[3 \, m^2 \, \frac{(B_n \, IF)}{2 \, F_v} \right] + C/N_i \text{dB} + DWL$$

Where:

$$m = \frac{\text{Peak Dev.}}{F_v} = \frac{10 \text{ MHz}}{4.2 \text{ MHz}} = 2.38$$

F_v = Highest video frequency = 4.2 MHz

B_nIF = IF noise bandwidth = 30 MHz

DWL = Deemphasis, Weighting Improvement, luminance and peak-to-peak to RMS correction factors = 18.9 dB

Therefore:

$$S/N_v dB = 36.73 \text{ dB} + C/N_i dB$$

The point where the measured S/N departs by 1 dB from the FM improvement curve, defines the static threshold characteristics. The static threshold should occur at a C/N_i of less than 8 dB. This result also shows that the receiver AGC dynamic range is greater than 15 dB. This is true since the AGC action maintains a constant signal level into the demodulator phase detector. If the AGC dynamic range is less than 15 dB, the measured noise level at the video output would vary non-linearily with C/N_i before threshold is reached and a degraded and erroneous static threshold measurement would result.

4.1.3 Dynamic Threshold

Connect the video input level of the transmitter to the Tektronix color bar generator, model 146. Adjust the transmitter output level via the attenuator to provide the receiver with an input level of -72 dBm.

Connect the receiver video output signal to the video test rack (see Figure 4-2). Observe the color bar pattern on the Tektronix matrix monitor.

Adjust the transmitter output level downward until impulses at a rate of 1 to 5 per second are observed on the color bar pattern. The on-set of these impulses is the receiver dynamic threshold point and can be determined by referring to the previously calibrated C/N_i, as a function of reciever input level. This threshold point should occur at a C/N_i of 11 dB or less. Record data.

4.1.4 Signal-to-Hum Ratio

Increase the input signal level to the receiver to -72 dBm. Connect the video output of the receiver to an oscilloscope through a 1 KHz low pass filter. The low pass filter used here is an active filter with a 75Ω input impedance, 0.1 dB cut off at 1 KHz, 60 dB rejection at 15.75 KHz (the sync pulse rate), unity gain below 1 KHz, and the output is a low output impedance voltage source. For this test, the test transmitter is modulated by an all black picture signal. This is necessary to introduce the sync pulses at the 15.75 KHz rate so that the clamping circuit is engaged for dc restoration. This results in a valid measurement since the clamping circuit is engaged during normal video performance. The peak-to-peak receiver hum level is measured at the mid-portion of the field time interval on the oscilloscope as shown in Figure 4-3.

Measure the receiver hum level as indicated on the oscilloscope. This level should be less than 3.16 mV. Record this level. Note that 50 dB below IV P-P is 3.16 mV.

4.2 BASEBAND PARAMETERS

4.2.1 Video Response

The video response will be measured by utilizing the standard television test signals. These tests will consist of the multiburst test signal,

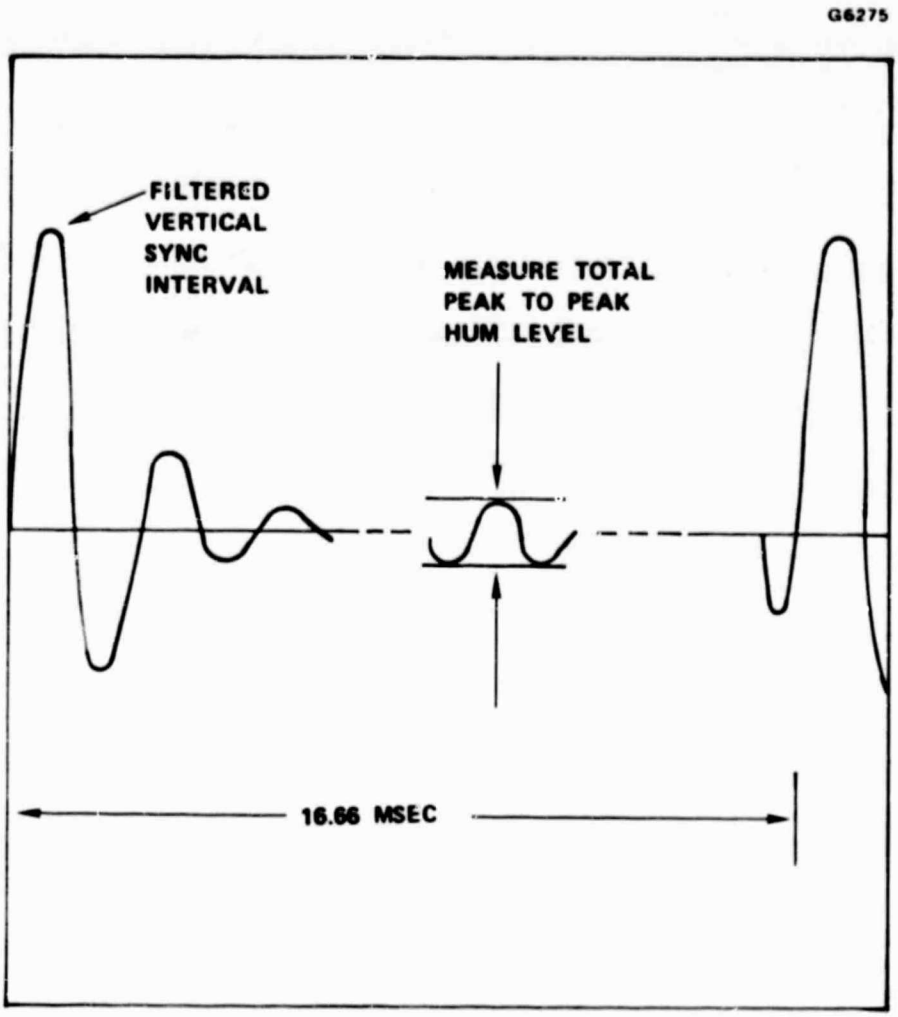


Figure 4-3 Receiver video hum level measurement on oscilloscope.

the field time, line time and short time test signals. Test results shall be recorded on the test data sheet. These tests will measure all of the following video parameters:

a. Deemphasis characteristics

b. Video response

c. Output level

d. Output sense

d. Clamping action.

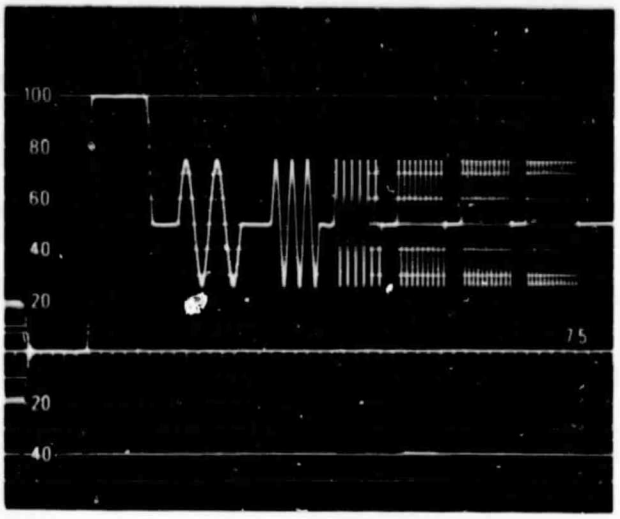
4.2.2 Gain/Frequency Distortion

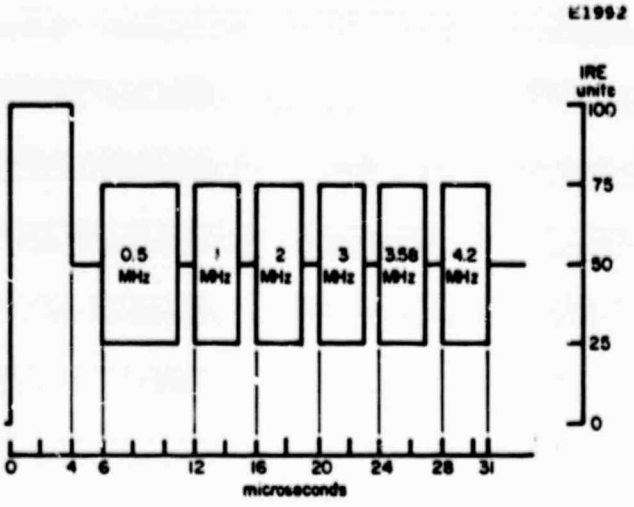
Definition

The gain/frequency distortion of a television facility is defined as the variation in gain over the frequency band extending from the television field repetition frequency to the nominal cutoff frequency of the facility, relative to the gain at a suitable reference frequency.

Measurement

The multiburst portion of the combination test signal shown in Figure 4-4 is used when measuring gain/frequency distortion in the range from 500 kHz to 4.2 MHz. The test signal's amplitude must be accurately adjusted at the sending end prior to the commencement of the test. Similarly the waveform monitor at the receiving end should be properly calibrated.





Generator Output Specifications

A) **White Flag**

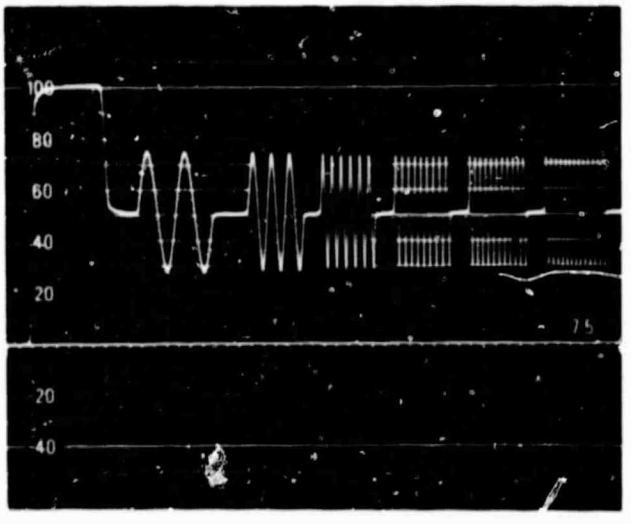
Peak amplitude	:	100 ± 1 IRE unit.
Time of rise and time of fall of flag edges	:	derived from the shaping network of the 2T sine-squared pulse.
Overshoot	:	less than ± 1 IRE unit.
Tilt	:	less than ± 1 IRE unit.

B) **Multiburst Frequencies**

All half-amplitude points of all burst frequencies	:	50 ± 1 IRE unit.

(The starting point of each burst frequency shall be at zero phase of each sinewave.)

Peak-to-peak amplitude of all bursts	:	50 ± 0.5 IRE units.



In this example, high frequency roll-off is shown. The burst amplitudes vary from 50 IRE units in the 500 kHz burst to 42 IRE units in the 4.2 MHz burst.

Figure 4-4 Gain/frequency distortion.

Following the above, the amplitude of the white flag should be adjusted to exactly 100 IRE units and then the peak-to-peak amplitude of each burst frequency should be measured and recorded. An example of gain/frequency distortion is shown in the lower illustration of Figure 4-3.

Performance Objective

With the white flag amplitude adjusted to 100 IRE units:

a. All frequency burst amplitudes shall be 50 ± 3 IRE units.

b. Color burst amplitude shall be 40 ± 4 IRE units.

NOTE: The performance objective shown above applies equally to both full-field and in-service VITS measurements.

4.2.3 Field-Time Waveform Distortion

Definition

When a television test signal having a period of one television field and of reference white amplitude is applied to the sending end of a television facility, the field-time waveform distortion is defined as the change in shape of the top of the test signal at the receiving end. The beginning and end of the test signal, equivalent to a few scanning lines, are excluded from the measurement.

Measurement

The field bar test signal shown in Figure 4-5 is used when measuring field-time waveform distortion. The test signal' amplitude must be

accurately adjusted at the sending end prior to the commencement of the test. Similarly the waveform monitor at the receiving end should be properly calibrated.

Following the above, the magnitude of the distrotion is obtained by measuring, in IRE units, the peak-to-peak change in amplitude of the bar top with the amplitude of the bar center adjusted to 100 IRE units. In order to avoid leading and trailing overshoots, the first and last 250 microseconds (approximately four television lines) are ignored in this measurement. An example of field-time waveform distortion is shown in the lower illustration of Figure 4-5.

Performance Objective

The peak-to-peak excursions of the bar top shall not exceed 2 IRE units.

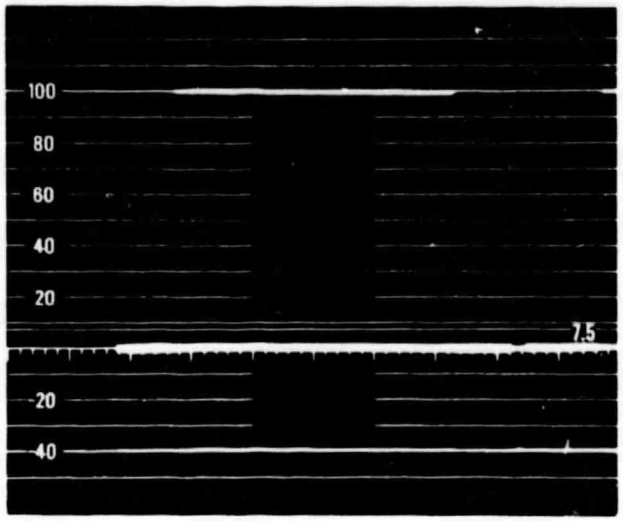
4.2.4. Line-Time Waveform Distortion

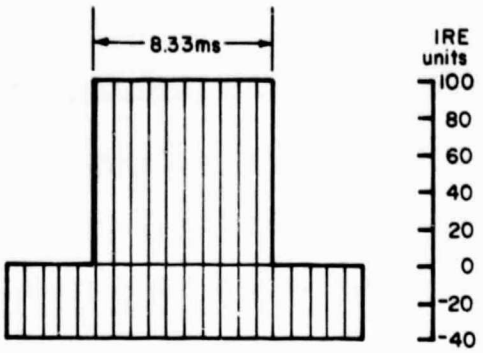
Definition

When a television test signal having a period of one television line and of reference white amplitude is applied to the sending end of a television facility, the line-time waveform distortion is defined as the change in shape of the top of the test signal at the receiving end. The beginning and end of the test signal, equivalent to a few picture elements, are excluded from the measurement.

Measurement

The line bar test portion of the composite test signal shown in Figure 4-6 is used when measuring line-time waveform distortion. The test signal's amplitude must be accurately adjusted at the sending end prior to the commencement of the test. Similarly the waveform monitor at the receiving end should be properly calibrated.

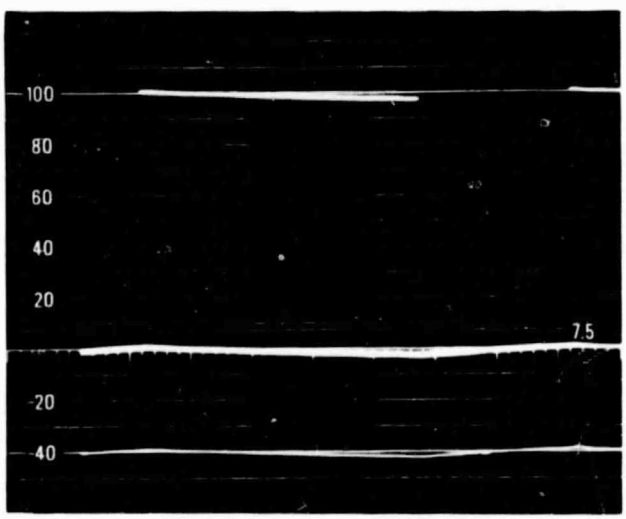




Generator Output Specifications

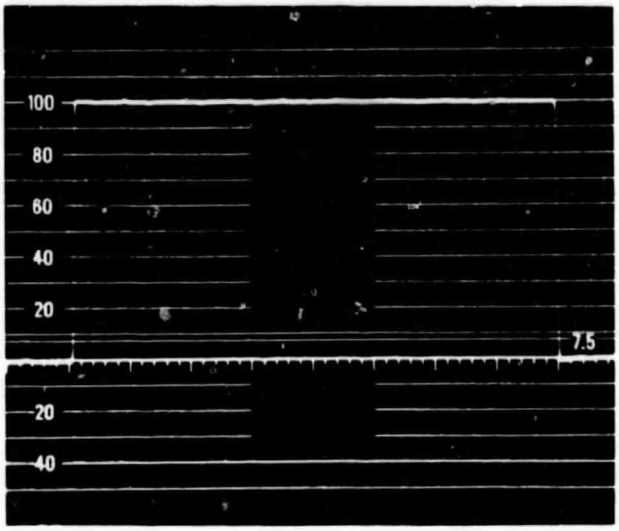
Peak amplitude of luminance signal	:	100 ± 0.5 IRE units
Peak amplitude of synchronizing signal	:	40 ± 0.5 IRE units
Field-time waveform distortion	:	less than 0.3 IRE units
Horizontal component	:	100 IRE unit flat field of 52.45 microsecond nominal duration

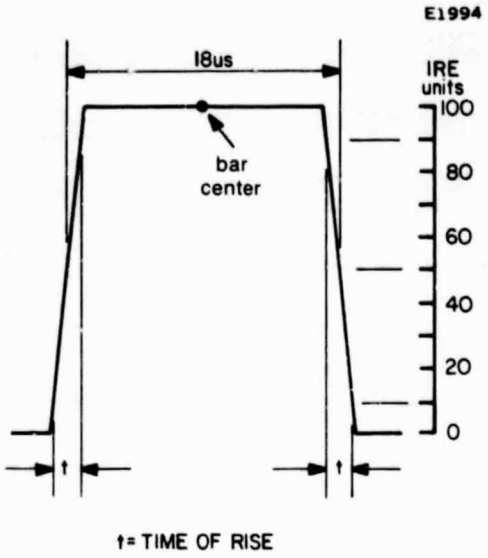
NOTE: This signal should be generated with field and line synchronizing pulses.



Field-Time Distortion is 3 IRE units. (+1, −2)

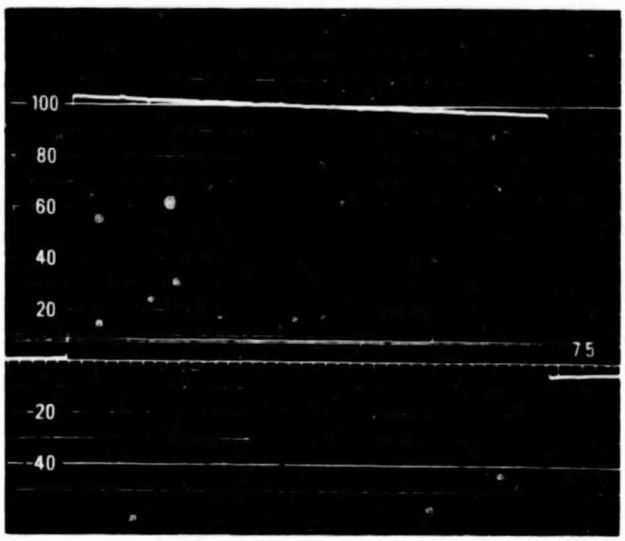
Figure 4-5 Field-time waveform distortion.





Generator Output Specifications

Peak amplitude	:	100 ± 0.5 IRE units
Line-time waveform distortion	:	less than 0.3 IRE units
Time of rise and time of fall of bar edges (10%-90%)	:	t = 125 ± 5 nanoseconds with integrated sine-squared shape



Line-Time Distortion is 4 IRE units. (+2, -2)

Figure 4-6 Line-time waveform distortion.

Following the above, the magnitude of the distortion is obtained by measuring, in IRE units, the peak-to-peak change in amplitude of the bar top with the amplitude of the bar center adjusted to 100 IRE units. The first and last one microsecond are ignored in this measurement. An example of line-time waveform distortion is shown in the lower illustration of Figure 4-6.

Performance Objective

The peak-to-peak excursions of the bar top shall not exceed 2 IRE units.

NOTE: The performance objective shown above applies equally to both full-field and in-service VITS measurements.

4.2.5 Short-Time Waveform Distortion

Definition

If a short pulse or rapid step function of reference white amplitude and defined shape is applied to the sending end of a television facility, the short-time waveform distortion is defined as the departure of the output pulse or step from its original shape. The choice of the half amplitude duration of the pulse or the rise-time of the step is determined by the nominal cutoff frequency of the television facility.

Measurement

The line bar portion of the composite test signal shown in Figure 4-7a and the 2T pulse test signal shown in Figure 4-6c are used when measuring short-time waveform distrotion. The test signal's amplitudes must be accurately adjusted at the sending end prior to the commencement of the test. Similarly the waveform monitor at the receiving end should be properly calibrated.

Following the above, the amplitude of the 2T pulse test signal is measured, in IRE units, having previously adjusted the amplitude of the line bar test signal to exactly 100 IRE units.

The peak-to-peak variations within the 1 microsecond intervals on either side (preceding and following) the T-step transitions (rise and fall) are then measured with the amplitude of the line bar test signal adjusted to 100 IRE units as measured between blanking and a point approximately 2 microseconds from the bar edge. (A graticule method of measuring short-time waveform distortion is currently under study by IEEE.) Examples of short-time waveform distortion are shown in Figures 4-6a and 4-7b.

Performance Objective

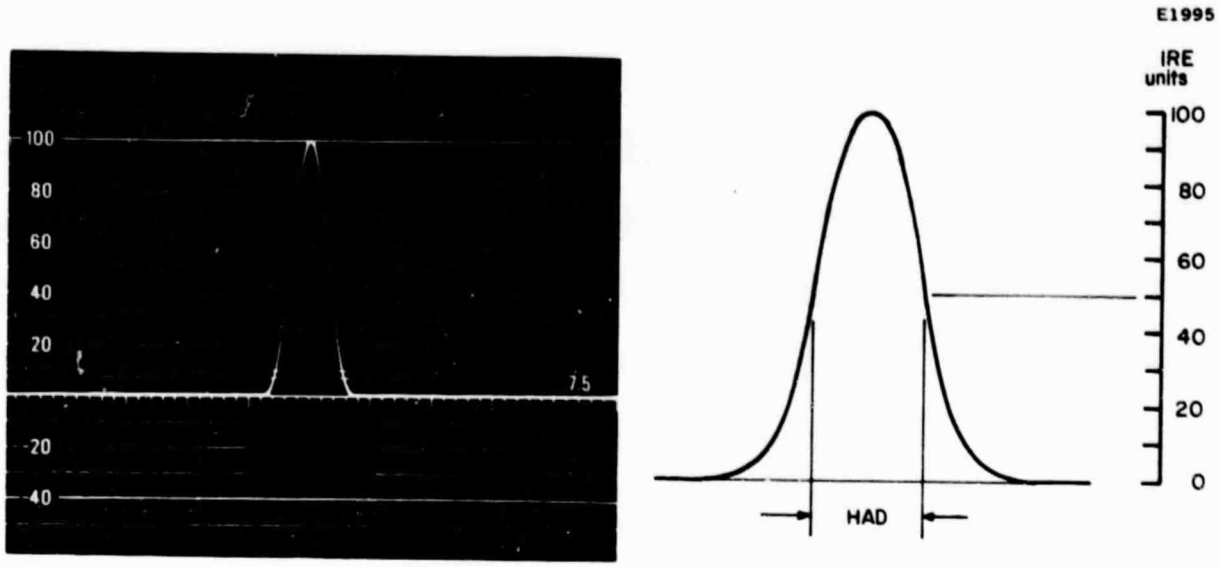
a. The 2T pulse amplitude shall be 100 ± 6 IRE units.

b. The peak-to-peak amplitude variations preceding or following the T-step transitions to the line bar test signal shall not exceed 2 IRE units.

NOTE: The performance objectives shown above apply equally to both full-field and in-service VITS measurements.

4.2.6 Impedance Level and Return Loss

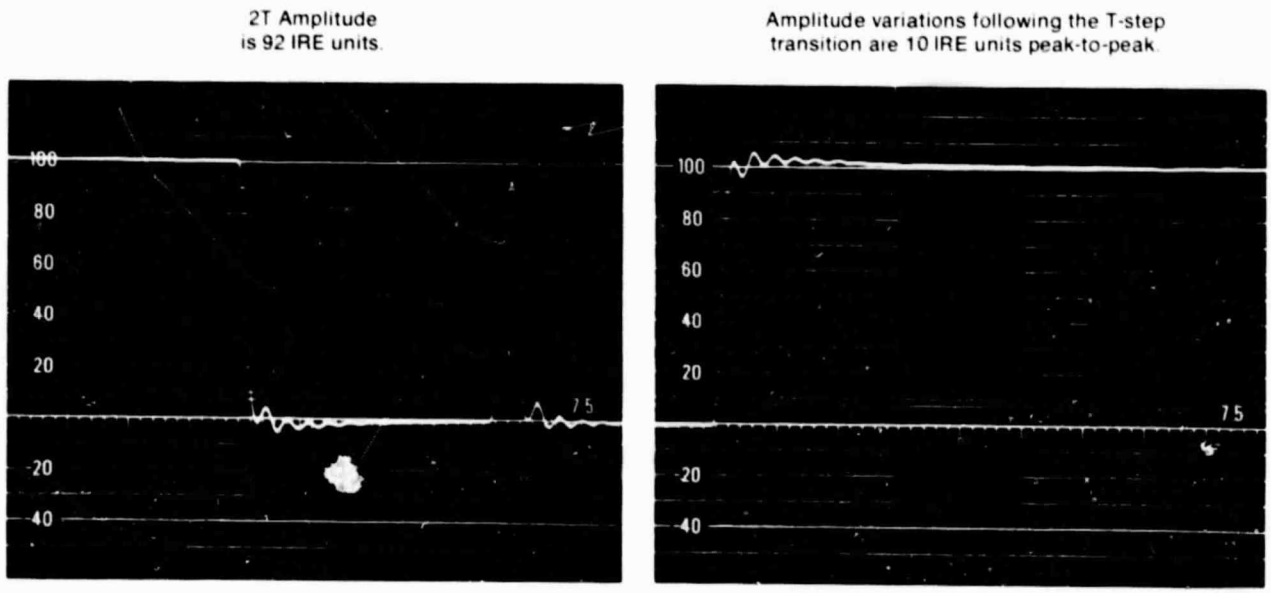
With the standard video modulated RF signal applied to the receiver, remove the 75 ohm termination from the waveform monitor and adjust the display for exactly 140 IRE units. Now terminate the waveform monitor with the standard 75 ohm termination. The output level as observed on



(c)

Generator Output Specifications

Peak amplitude	:	100 ± 0.5 IRE units
Half amplitude duration	:	250 ± 10 nanoseconds



(a) (b)

Figure 4-7 Short-time waveform distortion.

the display should be 70 ± 10 IRE units. This corresponds to an out impedance from 53 Ω to 107 Ω and a return loss greater than 15 dB. Record your results. Readjust the video level to 140 IRE units.

4.2.7 Differential Gain

Definition

If a small constant amplitude of chrominance subcarrier superimposed on a luminance signal, is applied to the sending end of a television facility, the differential gain is defined as the change in amplitude of the subcarrier at the receiving end as the luminance varies from blanking level to white level, the average picture level being maintained at a particular value.

Measurement

The modulated 5-riser staircase portion of the composite test signal shown in Figure 4-8 is used when measuring differential gain. The test signal's amplitude at each step level must be accurately adjusted at the sending end prior to the commencement of the test. Similarly the waveform monitor at the receiving end should be properly calibrated.

Following the above, the test signal should be fed through a high-pass filter network* and the output of the network connected to the waveform monitor being used for the measurement. The gain of the waveform monitor is then adjusted until the highest subcarrier peak-to-peak amplitude is exactly 100 IRE units. The peak-to-peak amplitude of the lowest subcarrier is then measured. The difference between the highest subcarrier amplitude and the lowest subcarrier amplitude is the differential gain distortion at 50 percent APL. The above measurement procedure

should be repeated using the same test signal transmitted on every fifth television line with intermediate lines set at blanking level for a 10 percent APL value and then at peak white level for a 90 percent APL value. The maximum differential gain distortion m measured should be recorded.

An example of differential gain distortion using the waveform monitor is shown in Figure 4-8.

Alternatively, the differential gain can be measured using an NTSC Vector Scope, Tektronix Model 520A to result in a finer resolution in the differential gain measurement. This method does not display the subcarrier directly; instead, linear envelope detection is used to produce a display as shown in Figure 4-8. To make this measurement, the vector display must be used to adjust sensitivity of the vectorscope.

Performance Objective

At 10 percent, 50 percent, and 90 percent APL the differential gain shall not exceed 2 percent (2 IRE units).

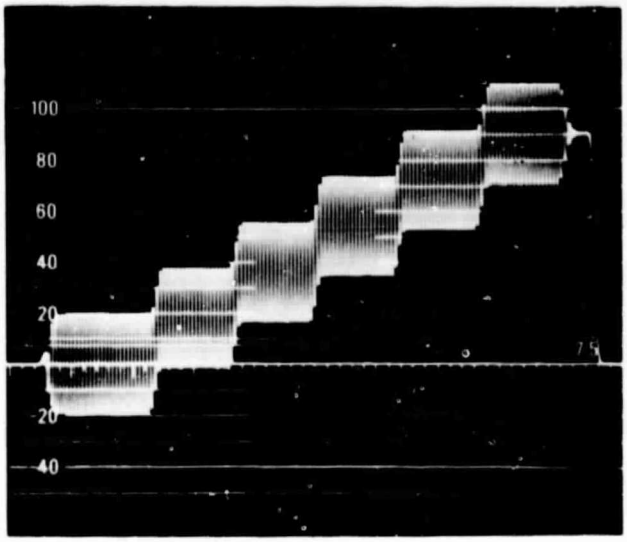
NOTE: The performance objective shown above also applies to the in-service VITS measurement.

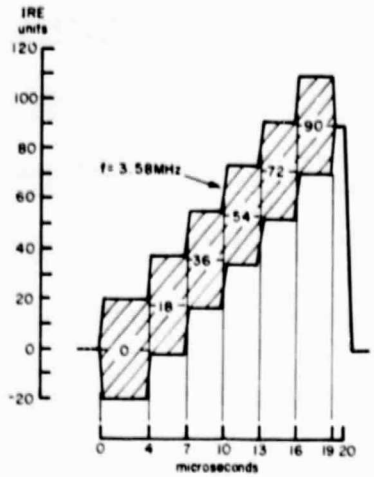
4.2.8 Differential Phase

Definition

If a constant amplitude of chrominance subcarrier without phase modulation, superimposed on a luminance signal, is applied to the sending end

*The chroma filter network incorporated into most television waveform monitors is suitable for this test.

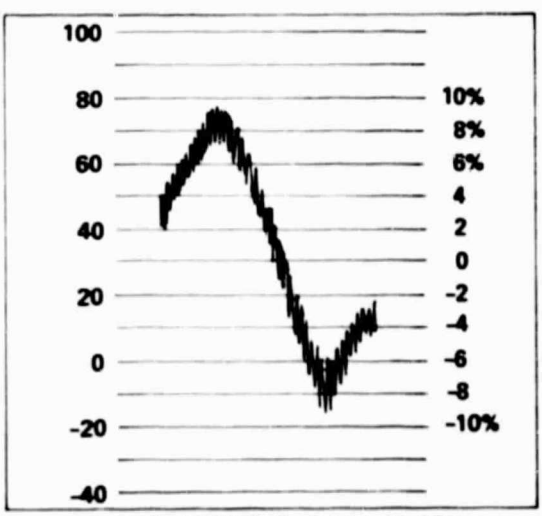




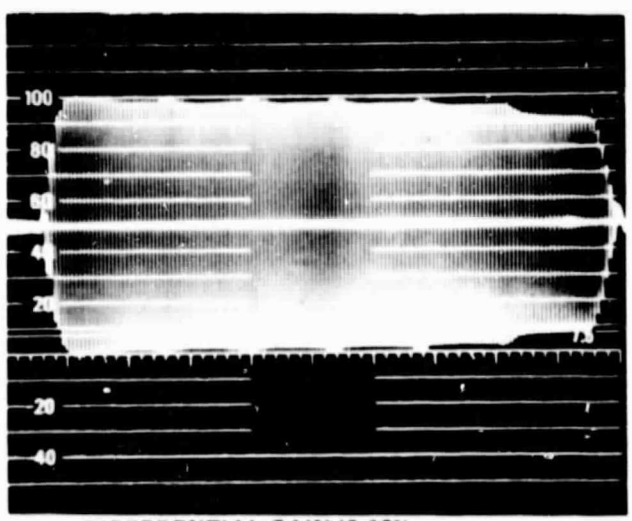
Generator Output Specifications

(In addition to the luminance specifications shown with Figure 20 in Section 3.9)

Chrominance amplitude	:	40 ± 0.5 IRE units
Inherent differential gain	:	less than 0.5 percent
and differential phase	:	less than 0.2°
Rise and fall times of the modulation envelope	:	400 ± 25 nanoseconds
Phase of chrominance signal relative to reference burst phase	:	0° ± 1.0° over the range 10% to 90% APL



DIFFERENTIAL GAIN IS 16%
MEASURED WITH VECTOR SCOPE



DIFFERENTIAL GAIN IS 16%.
MEASURED WITH WAVEFORM MONITOR

FIGURE 4-8 DIFFERENTIAL GAIN.

of a television facility, the differential phase is defined as the change in the phase of the subcarrier at the receiving end as the luminance varies from blanking level to white level, the average picture level being maintained at a particular value.

Measurement

The modulated 5-riser staircase portion of the composite test signal shown in Figure 4-8 is used when measuring differential phase. The test signal's amplitude and its subcarrier phase at each step level must be accurately adjusted at the sending end prior to the commencement of the test. Similarly the waveform monitor and phase comparator (e.g., vectorscope) at the receiving end should be properly calibrated. A vectorscope display of differential phase with zero distortion is shown in Figure 4-9a.

Following the above, the test signal should be fed through a high-pass filter network to the phase comparator (or directly to the vectorscope). The differential phase distortion is the measured peak-to-peak change in subcarrier phase at 50 percent APL. The above measurement procedure should be repeated using the same test signal transmitted on every fifth television line with intermediate lines set at blanking level for a 10 percent APL value and then at peak white level for a 90 percent APL value. The maximum differential phase distortion should be recorded.

An example of differential phase distortion is shown in Figure 4-9b.

Performance Objective

At 10 percent, 50 percent, and 90 percent APL the differential phase shall not exceed 1 degree.

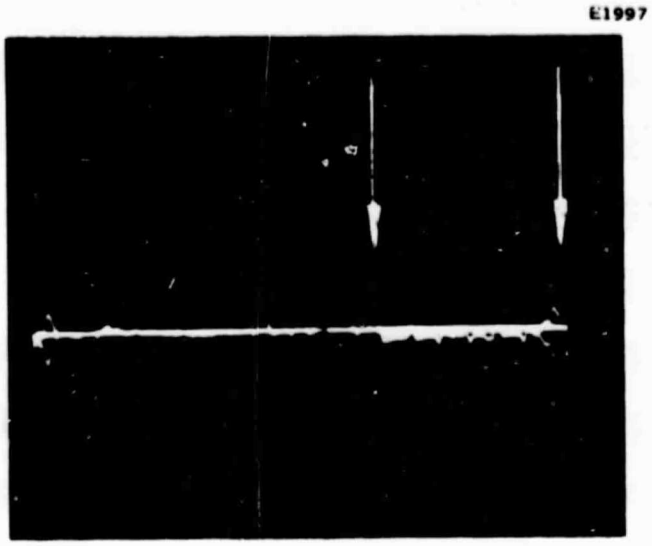


Figure 4-9a Zero differential phase distortion.

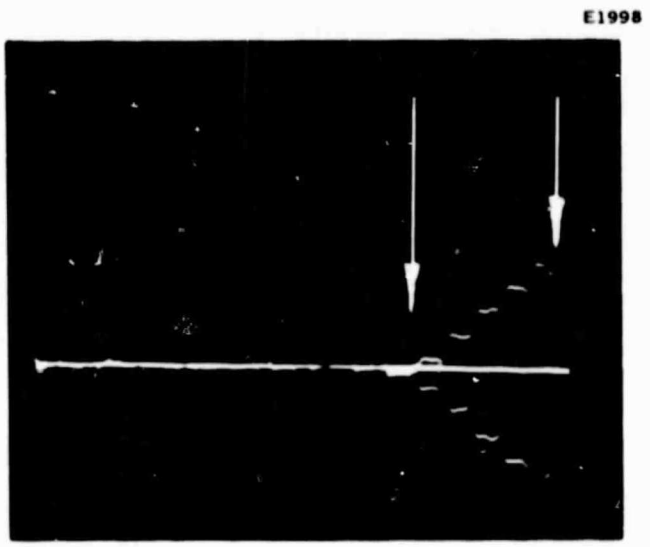


Figure 4-9b Differential phase distortion.

NOTE: The performance objective shown above also applies to the in-service VITS measurement.

4.2.9 Chrominance-Luminance Gain Inequality

Definition

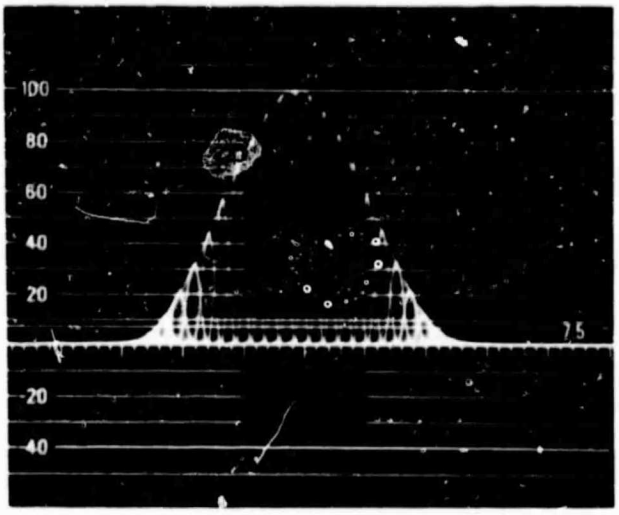
When a test signal having defined luminance and chrominance components is applied to the sending end of a television facility, the chrominance-luminance gain inequality is defined as the change in amplitude at the receiving end of the color component of the test signal relative to the luminance component.

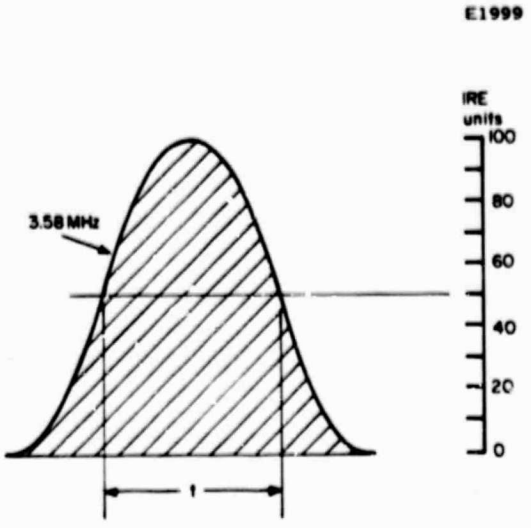
Measurement

The chrominance pulse portion of the composite test signal shown in Figure 4-10a is used when measuring chrominance-luminance gain inequality.* The test signal's amplitude must be accurately adjusted at the sending end prior to the commencement of the test. Similarly the waveform monitor at the receiving end should be properly calibrated.

Following the above, the amplitude of the Chrominance Pulse Test Signal is measured in IRE units, having previously adjusted the amplitude of the line bar test signal to exactly 100 IRE units. This method is accurate to within 2 percent with up to 300 nanoseconds of chrominance-to-luminance delay present. The convention of Figure 4-10b shows how the chrominance pulse will look with different types of gain and delay distortion. If harmonic distortion is present on the chroma pulse, as

*This parameter is also called Relative Chroma Level (RCL), and is expressed as a percentage of P-P chrominance referenced to the line bar amplitude, as shown in Figure 4-10a. Hence, the performance objective expressed as RCL would be ±6 percent.





Generator Output Specifications

Peak amplitude	:	100 ± 0.5 IRE units
Half amplitude duration	:	t = 1562.5 ± 50 nanoseconds
Inherent chrominance luminance		
a) gain inequality (RCL)	:	less than ± 0.5 IRE (± 1%)
b) delay inequality (RCT)	:	less than 5 nanoseconds, delayed or advanced
Subcarrier harmonic distortion	:	less than 1%
Irregularities in the pulse base line	:	less than ± 0.5 IRE units

Figure 4-10a The chrominance pulse test signal.

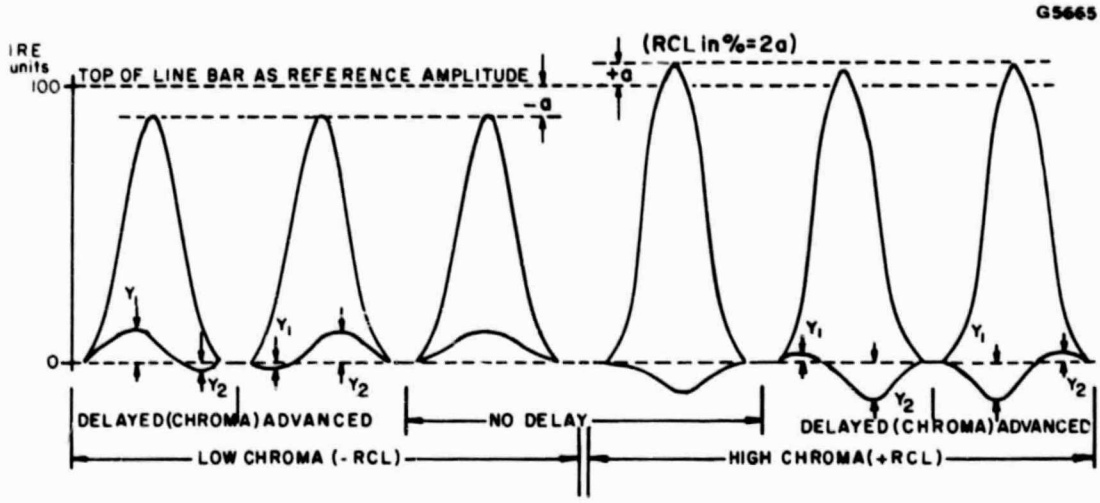


Figure 10b Chrominance-luminance gain measurement convention.

evidenced by multiple irregularties of the baseline, this method is invalid and an accurate measurement cannot be made. Methods to make measurements in the presence of harmonic distortion are presently under study.

An example of low chrominance amplitude is shown in Figure 4-10c.

Performance Objective

The amplitude of the chrominance pulse shall be 100 ± 3 IRE units.

NOTE: The performance objective shown above applies equally to both full-field and in-service VITS measurements.

4.2.10 Chrominance-Luminance Delay Inequality

Definition

When a test signal having defined luminance and chrominance components is applied to the sending end of a television facility, the chrominance-luminance delay inequality is defined as the change in relative timing, at the receiving end, of the chrominance component of the test signal relative to the luminance component.

Measurement

The chrominance pulse portion of the composite test signal shown in Figure 4-10a is used when measuring chrominance-luminance delay inequality.* The test signal's amplitude must be accurately adjusted at the sending end prior to the commencement of the test. Similarly the waveform monitor at the receiving end should be properly calibrated.

*This parameter is also called Relative Chroma Time.

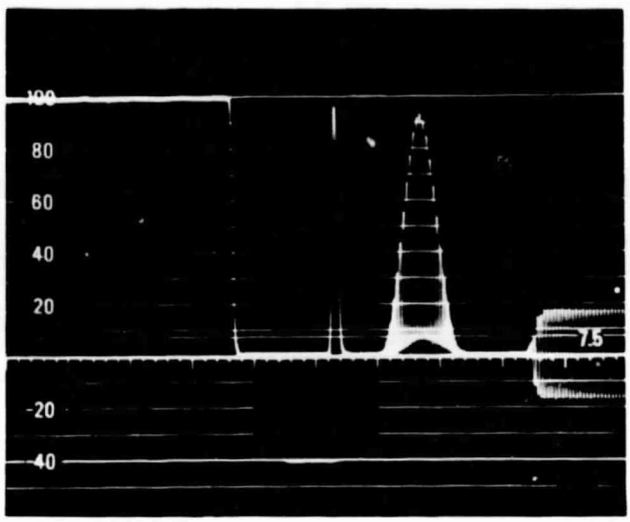


Figure 4-10c Example of low chrominance amplitude.

Following the above, the amplitude of the chrominance pulse test signal should be adjusted to exactly 100 IRE units. The nomogram shown in Figure 4-11a should be used to compute the magnitude of the chrominance-luminance delay inequality. If the chrominance component of the test signal starts with a positive going lobe then the chrominance-luminance delay inequality should be recorded as delayed chroma. The delay inequality can also be computer by the formula:

$$\text{CLDI(RCT) in ns} = 20\sqrt{Y_1 \cdot Y_2}.$$

If harmonic distortion is present, as evidenced by multiple irregularities of the baseline, this method is invalid and an accurate measurement cannot be made. Methods to determine chrominance-luminance delay inequality in the presence of harmonic distortion are currently under study.

An example of chrominance-luminance delay inequality is shown in Figure 4-11b below.

Performance Objective

The chrominance-luminance delay inequality shall be no greater than 50 nanoseconds, advanced or delayed chroma.

NOTE: The performance objective shown above applied equally to both full-field and in-service VITS measurements.

4.3 AUDIO SUBCARRIER PARAMETERS

The test equipment is set up as shown in Figure 4-12. In these tests, in addition to the standard video modulation on the RF signal, as described in section 4.1, the input RF signal is also modulated by the audio subcarrier.

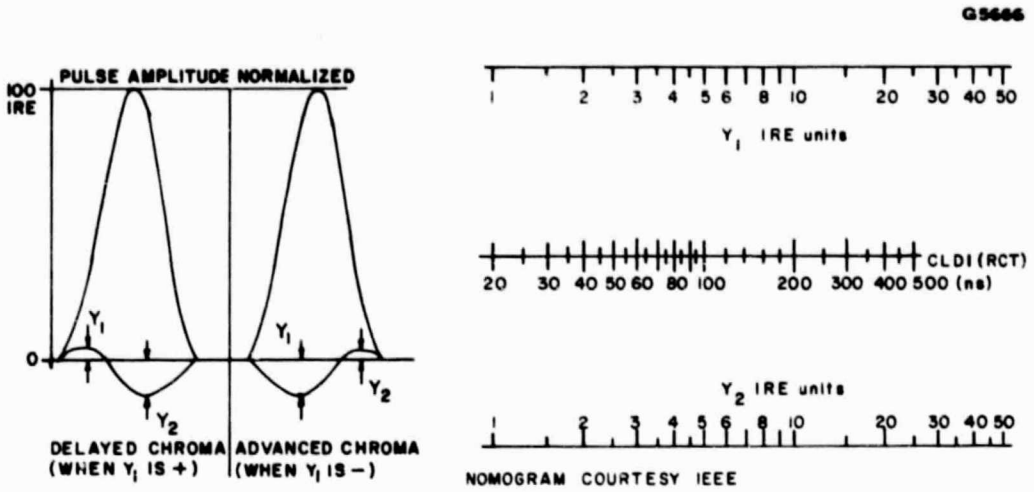


Figure 4-11a Chrominance-luminance delay nomogram with measurement convention.

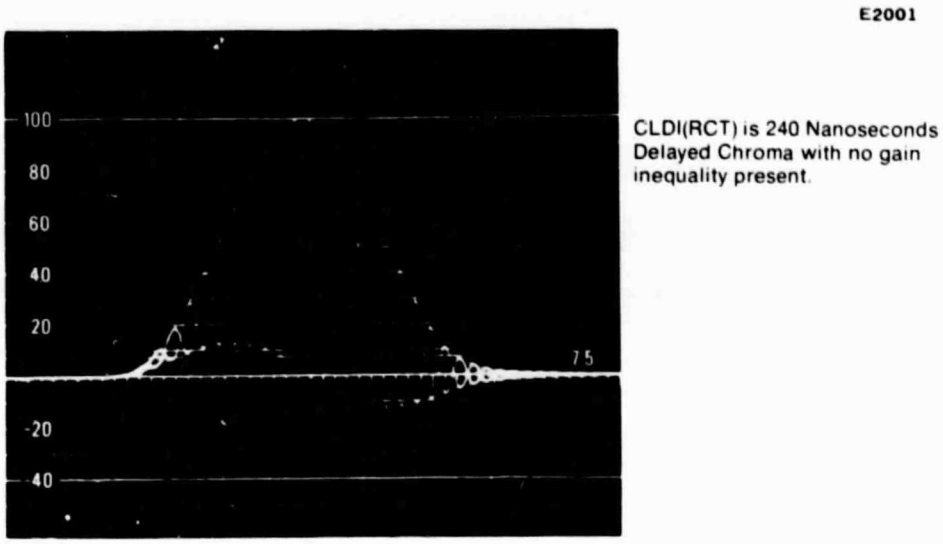


Figure 4-11b Chrominance-luminance delay inequality.

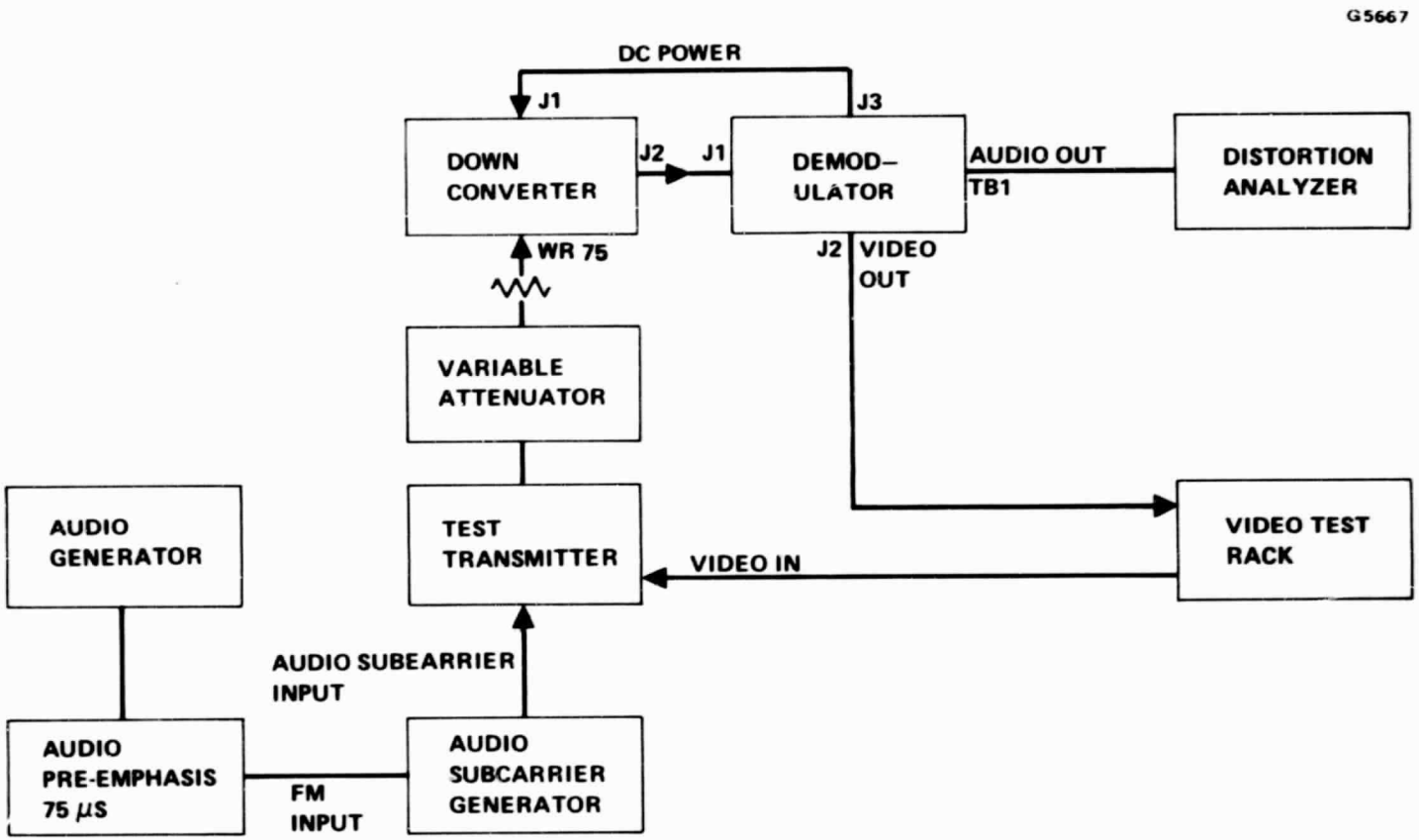


Figure 4-12 Audio measurement tests.

The audio subcarrier frequency is set to 5.140 MHz. The frequency of the audio signal generator is set between 30 Hz and 15 KHz and the level of the audio signal is adjusted to provide 60.0 KHz peak subcarrier deviation. The level of the subcarrier is adjusted for 630 KHz deviation of the main RF carrier. Check the video output of the Demodulator unit to make sure that the composite video test signal is present.

4.3.1 Output Level

Set the audio generator at 1 KHz. With the distortion analyzer input terminated in 600 ohms and with the switch on the distortion analyzer in the voltmeter function, set the displayed RMS voltage level to 0.778 volts, or 0 dBm.

4.3.2 Output Impedance and Return Loss

With the input impedance of the distortion analyzer set at infinity, note the voltage level indicated. This level should be 6 dB ±1.4 dB above the 0.778 volt level previously set. Record your results.

4.3.3 Frequency Response Flatness

With the audio frequency varied from 30 Hz to 15 KHz, note the voltage level indicated on the distortion analyzer (voltmeter function and input impedance at 600 Ω). Note and record the 3dB bandwidth response and the amplitude variation from 100 Hz to 10 KHz. The 3dB bandwidth should be 30 Hz to 15 KHz with maximum amplitude ripple of ±1 dB from 100 Hz to 10 Kz. Record your results.

4.3.4 Distortion

Modulate the transmitter with a standard color bar signal. Set the audio modulation frequency of the transmitter subcarrier to 1 KHz at

the proper deviation level. Adjust the RF input level to the receiver at a level of -72 dBm. Measure the distortion of the receiver audio output signal using the Distortion Measurement Set. The distortion should be less than 5%. Record your results.

4.3.5 Test Tone Signal-to-Noise Ratio

Adjust the RF input level to the receiver at a level of -80 dBm. All other parameters the same as for the distortion measurements. Set the Distortion Test Set to the voltmeter function, switch in the 30 KHz low pass filter and verify that the receiver output level is 0 dBm in 600 ohms. Switch the 1 KHz modulation applied to the transmitter to the off position. Now increase the voltmeter sensitivity on the Distortion Test Set until a reading is obtained. This level should be greater than 45 dB below the test tone level. Record your results.

4.3.6 Static Threshold

Increase the RF input to the receiver to -72 dBm. Note the noise level indicated on the distortion test set and compute the signal-to-noise at this setting. Record your results. Repeat this procedure by adjusting the RF input signal to the receiver to the receiver downward in 1 dB steps until data has been obtained at a level of -87 dBm. The static threshold may now be obtained by plotting the audio signal-to-noise ratio vs. the receiver carrier-to-noise ratio. The point where the measured S/N departs by 1 dB from the straight line plot indicates the static threshold. This point should occur at a C/N_i of less than 10 dB. Record your results.

Test Data Summary

12 GHz Satellite Video Receiver

Serial Number _____ Date _____

Performed by _____ Approved _____

Functional Tests

Ref. Para.	Description	Specification	Test Results
Downconverter Tests			
3.1	Down Converter Gain	52 ±6 dB	_____
3.2	Local Osc. Stability	±4.0 MHz	_____
3.3	RF Input VSWR	2:1 max	_____
3.4	Image Rejection	15 dB min	_____
3.5	Receiver NF	4 dB max	_____
Demodulator RF Tests			
4.1.2	Static Threshold	C/Ni < 8 dB	_____
	Signal-to-Noise Weighted at C/N: = 12 dB	48.5 dB min	_____
4.1.3	Dynamic Threshold	C/Ni < 11 dB	_____
4.1.4	Signal-to-Hum Ratio	50 dB min	_____
Video Baseband Parameters			
4.2.2	Gain Frequency Distortion	50 ±3 IRE	_____
4.2.3	Field Time Distortion	±2 IRE	_____
	Line Time Distortion	±2 IRE	_____
	Short Time Distortion	100 ±6 IRE	_____
4.2.6	Impedance Level and Return Loss	70 ±10 IRE	_____
4.2.7	Differential Gain	2%	_____
4.2.8	Differential Phase	1 degree	_____
4.2.9	Chrominance-Luminance Gain	100 ±3 IRE	_____
4.2.10	Chrominance-Luminance Delay	50 ns	_____

Ref. Para.	Description	Specification	Test Results
Audio Baseband Parameters			
4.3.2	Output Impedance and Return Loss	6 dB ± 1.4 dB	_____
4.3.3	Frequency Response Flatness	30 HZ-15 KHz, 3 dB 100 HZ-10 KHz, 1 dB	_____ _____
4.3.4	Distortion	5% max	_____
4.3.5	Test Tone Signal-to-Noise	45 dB min	_____
4.3.6	Static Threshold	C/N_i < 10 dB	_____